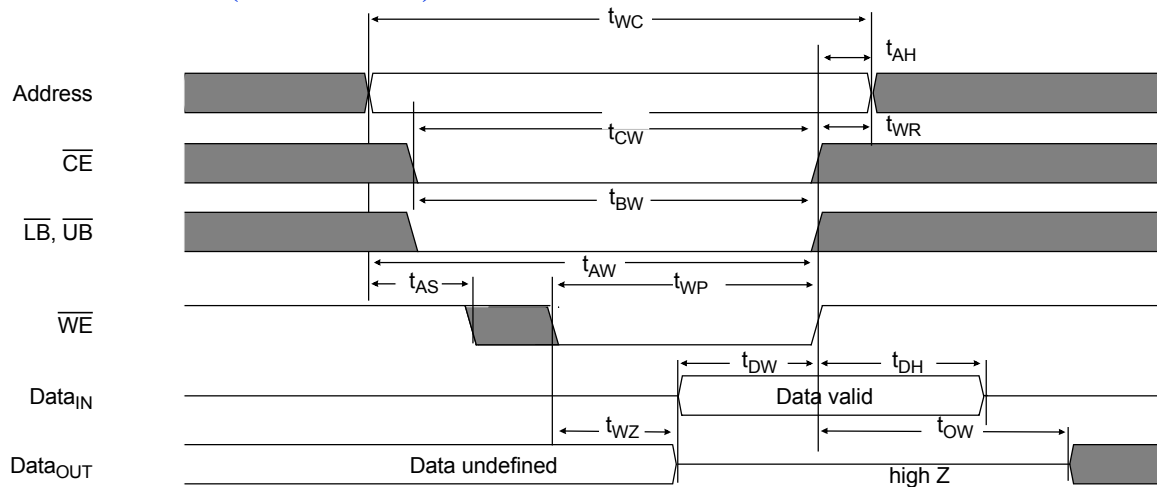




Write cycle (over the operating range) ¹¹

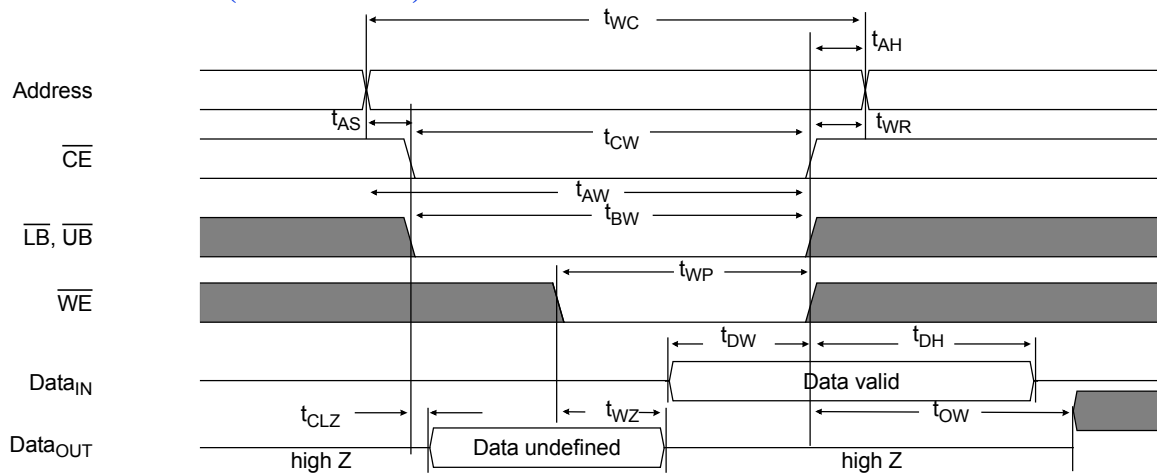
Parameter	Symbol	AS7C31026C-12		Unit	Notes
		Min	Max		
Write cycle time	t_{WC}	12	–	ns	
Chip enable (\overline{CE}) to write end	t_{CW}	8	–	ns	
Address setup to write end	t_{AW}	8	–	ns	
Address setup time	t_{AS}	0	–	ns	
Write pulse width	t_{WP}	8	–	ns	
Write recovery time	t_{WR}	0	–	ns	
Address hold from end of write	t_{AH}	0	–	ns	
Data valid to write end	t_{DW}	6	–	ns	
Data hold time	t_{DH}	0	–	ns	5
Write enable to output in high Z	t_{WZ}	–	6	ns	4, 5
Output active from write end	t_{OW}	3	–	ns	4, 5
Byte select low to end of write	t_{BW}	8	–	ns	

Write waveform 1 (\overline{WE} controlled) ^{10,11}





Write waveform 2 (\overline{CE} controlled)^{10,11}



AC test conditions

- Output load: see Figure B.
- Input pulse level: GND to 3.0 V. See Figure A.
- Input rise and fall times: 3 ns. See Figure A.
- Input and output timing reference levels: 1.5

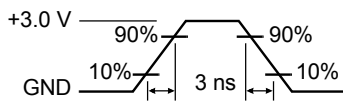


Figure A: Input pulse

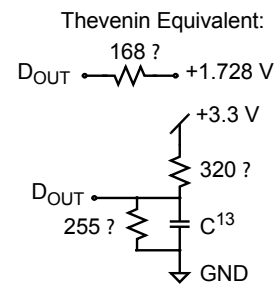


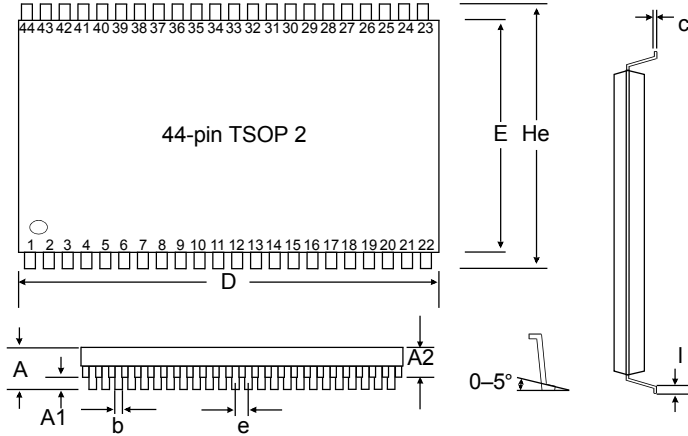
Figure B: 3.3 V Output load

Notes

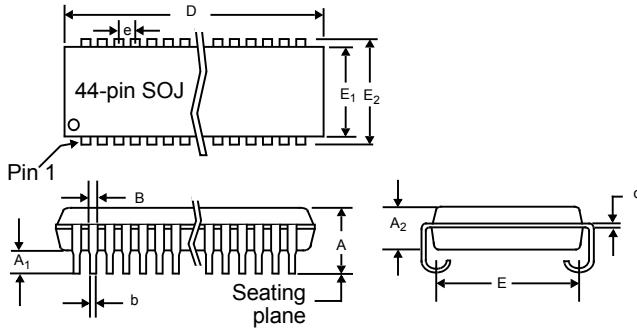
- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see *AC Test Conditions*, Figures A and B.
- 4 These parameters are specified with $C_L = 5$ pF, as in Figures B. Transition is measured ± 200 mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6 \overline{WE} is high for read cycle.
- 7 \overline{CE} and \overline{OE} are low for read cycle.
- 8 Address is valid prior to or coincident with \overline{CE} transition low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 N/A
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 Not applicable.
- 13 $C = 30$ pF, except all high Z and low Z parameters where $C = 5$ pF.



Package dimensions



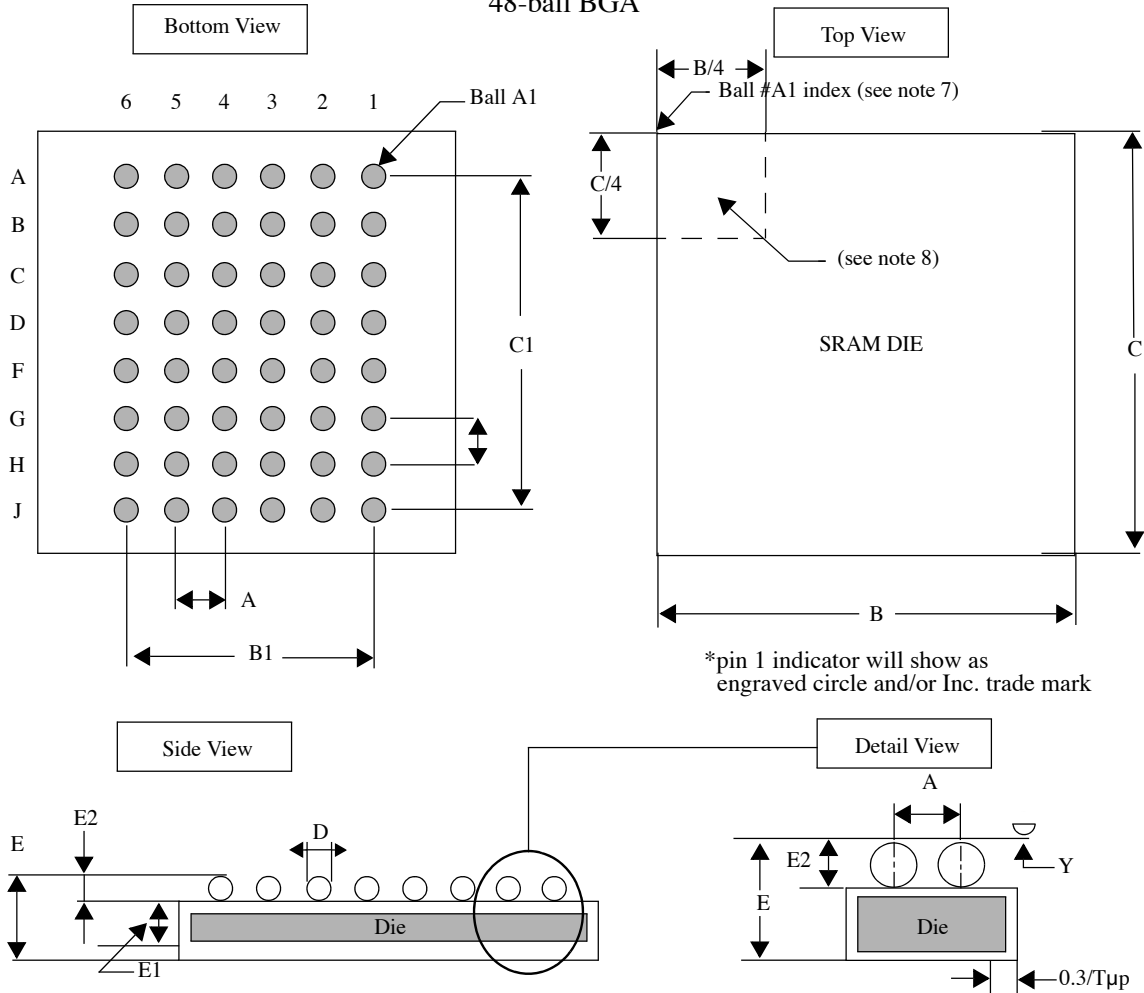
	44-pin TSOP 2	
	Min (mm)	Max (mm)
A		1.2
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.120	0.21
D	18.31	18.52
E	10.06	10.26
He	11.68	11.94
e	0.80 (typical)	
I	0.40	0.60



	44-pin SOJ 400 mil	
	Min (in)	Max (in)
A	0.128	0.148
A1	0.025	-
A2	0.105	0.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	0.435	0.445
e	0.050 NOM	



48-ball BGA



*pin 1 indicator will show as engraved circle and/or Inc. trade mark

	Minimum	Typical	Maximum
A	–	0.75	–
B	6.00 BSC		
B1	–	3.75	–
C	8.00 BSC		
C1	–	5.25	–
D	0.25	0.30	0.40
E	1.14	1.24	1.34
E1	–	0.68	–
E2	0.15	0.20	0.25
Y	–	–	0.010

Notes

- 1 Bump counts: 48 (8 row x 6 column).
- 2 Pitch: (x,y) = 0.75 mm x 0.75 mm (typ).
- 3 Units: millimeters.
- 4 All tolerance are +/- 0.050 unless otherwise specified.
- 5 Typ: typical.
- 6 Y is coplanarity: 0.010 (max).
- 7 "A1" ID corner must be identified by chamfer, ink mark, metallized marking, indentation or other feature on the package body.
- 8 If "A1" ID corner is on the package body, it must be located within the zone indicated.

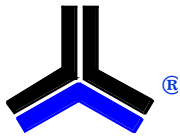


Ordering codes

Package	Volt/Temp	12 ns
Plastic SOJ, 400 mil	3.3V industrial	AS7C31026C-12JIN
TSOP 2, 10.2 x 18.4 mm	3.3V industrial	AS7C31026C-12TIN
BGA, 7 x 7 mm	3.3V industrial	AS7C31026C-12BIN

Part numbering system

AS7C	X	1026B	-XX	X	X	X
SRAM prefix	Voltage: 3 = 3.3 V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP 2, 10.2 x 18.4 mm B=BGA, 7 x 7 mm	Temperature I = industrial: -40° C to 85° C	N = Lead Free Part



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Part Number: AS7C31026C-12JIN

Document Version: v 2.0

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