## Revision History AS4C64M16D1 – 66-pin TSOP II package

| Revision | Details | Date |
|---|---|---|
| Rev 1.0 | Preliminary datasheet | Sep 2014 |
| Rev 2.0 | Speed grade option changed -5(200MHz) to -6(166MHz) | Oct 2014 |
| Rev 2.1 | Revise the speed information about DDR-400 or 200MHZ | Mar 2023 |

# 64M x 16 bit DDR1 Synchronous DRAM (SDRAM)

**Confidential** **Advanced (Rev. 2.1, Mar. /2023)**

### Features

High speed data transfer rates with system frequency up to 166MHz

- Data Mask for Write Control
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2, 2.5, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 2, 4, 8 for Sequential Type 2, 4, 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64 ms
- Available in 66 Pin TSOP II
- SSTL-2 Compatible I/Os
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQS) for input and output data, active on both edges
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- Differential clock inputs CK and $\overline{CK}$
  VDD = 2.5V ± 0.2V, VDDQ = 2.5V ± 0.2V
  tRAS lockout supported
  Concurrent auto precharge option is supported

**All parts are ROHS compliant**

### Description

The AS4C64M16D1 is a four bank DDR DRAM organized as 4 banks x 16Mbit x 16. The AS4C64M16D1 achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

All of the controls, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are occurring on both edges of DQS.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, $\overline{CAS}$ latency and speed grade of the device.

| | **-6** |
|---|---|
| | DDR333 |
| Clock Cycle Time ($t_{CK2}$) | 7.5ns |
| Clock Cycle Time ($t_{CK2.5}$) | 6ns |
| Clock Cycle Time ($t_{CK3}$) | 6ns |
| System Frequency ($f_{CK\ max}$) | 166 MHz |

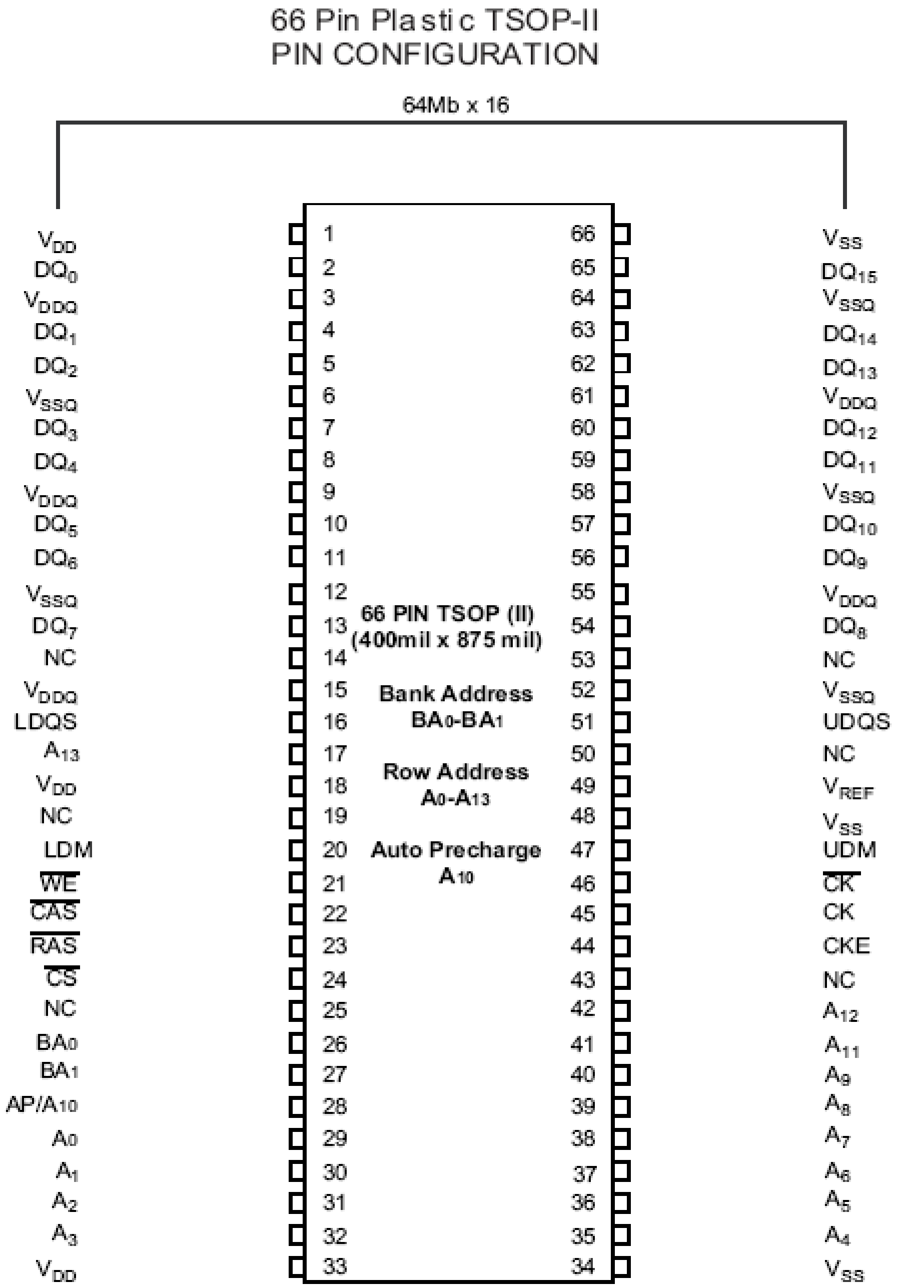
## Table 1. Speed Grade Information

| Speed Grade | Clock Frequency | CAS Latency | $t_{RCD}$ (ns) | $t_{RP}$ (ns) |
|---|---|---|---|---|
| DDR1-333 | 166 MHz | 3 | 18 | 18 |

## Table 2. Ordering Information

| Product part No | Org | Temperature | Package |
|---|---|---|---|
| **AS4C64M16D1-6TCN** | **64M x 16** | **Commercial**<br>**0°C to 70°C** | **66-pin TSOP II** |
| **AS4C64M16D1-6TIN** | **64M x 16** | **Industrial**<br>**-40°C to 85°C** | **66-pin TSOP II** |

## *66 Pin Plastic TSOP-II PIN CONFIGURATION*

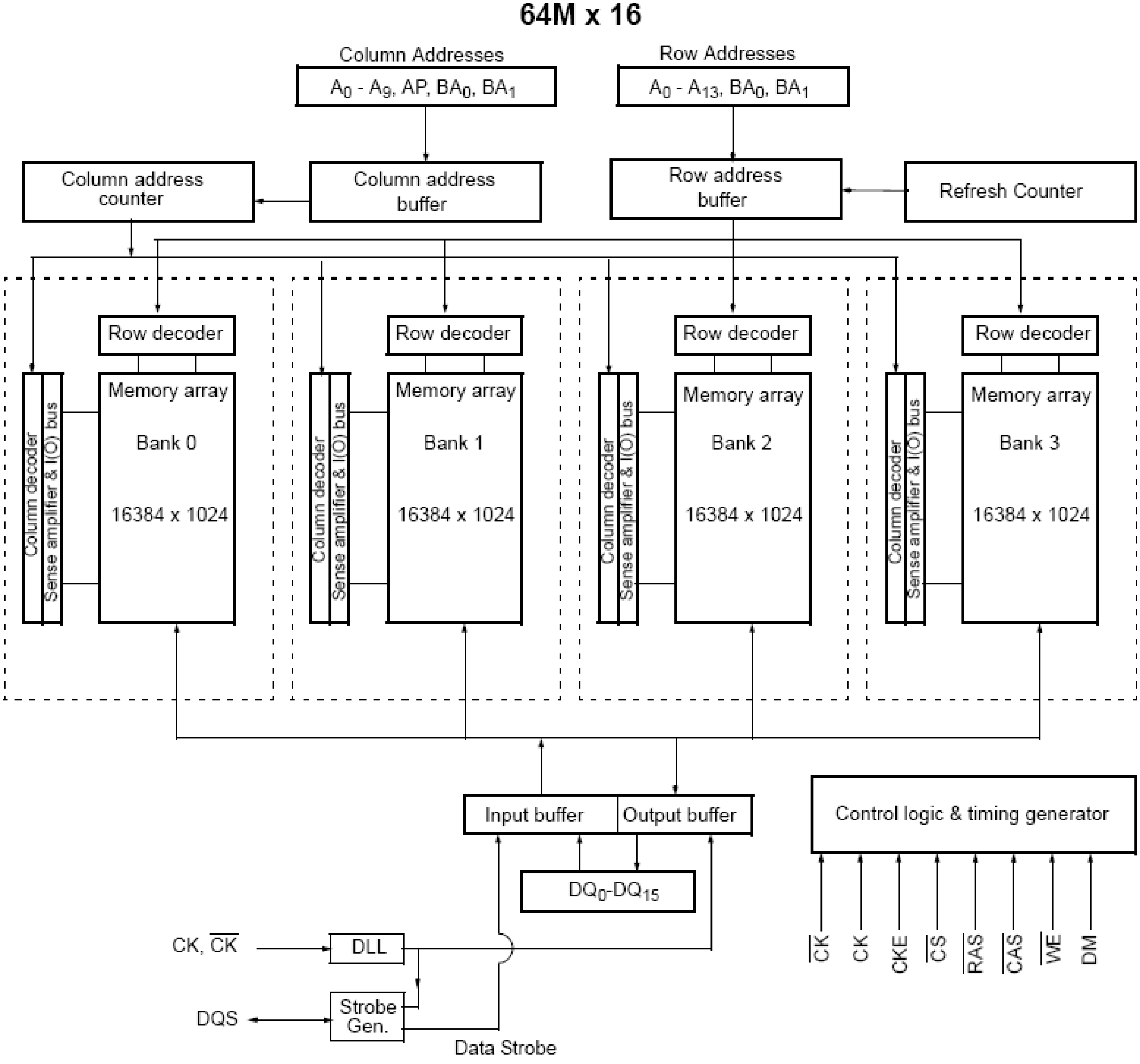


### Pin Names

| | |
|---|---|
| CK, $\overline{CK}$ | Differential Clock Input |
| CKE | Clock Enable |
| $\overline{CS}$ | Chip Select |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| DQS (UDQS, LDQS) | Data Strobe (Bidirectional) |
| $A_0$–$A_{13}$ | Address Inputs |
| $BA_0$, $BA_1$ | Bank Select |

| | |
|---|---|
| DQ's | Data Input/Output |
| DM (UDM, LDM) | Data Mask |
| $V_{DD}$ | Power<br>(+2.5V and +2.6V for DDR400) |
| $V_{SS}$ | Ground |
| $V_{DDQ}$ | Power for I/O's<br>(+2.5V and +2.6V for DDR400) |
| $V_{SSQ}$ | Ground for I/O's |
| NC | Not connected |
| $V_{REF}$ | Reference Voltage for Inputs |

## *Block Diagram*



### *Absolute Maximum Ratings**

| | |
|---|---|
| Operating temperature range | 0 to 70 °C for normal<br>-40 to 85 °C for Industrial |
| Storage temperature range | -55 to 150 °C |
| $V_{DD}$ Supply Voltage Relative to $V_{SS}$ | -1 V to +3.6 V |
| $V_{DDQ}$ Supply Voltage Relative to $V_{SS}$ | -1 V to +3.6 V |
| VREF and Inputs Voltage Relative to $V_{SS}$ | -1 V to +3.6 V |
| I/O Pins Voltage Relative to $V_{SS}$ | -0.5 V to $V_{DDQ}$ +0.5 V |
| Power dissipation | 1.6 W |
| Data out current (short circuit) | 50 mA |

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### *Signal Pin Description*

| Pin | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| CK<br>$\overline{\text{CK}}$ | Input | Pulse | Positive Edge | The system clock input. All inputs except DQs and DMs are sampled on the rising edge of CK. |
| CKE | Input | Level | Active High | Activates the CK signal when high and deactivates the CK signal when low, thereby initiates either the Power Down mode, or the Self Refresh mode. |
| $\overline{\text{CS}}$ | Input | Pulse | Active Low | $\overline{\text{CS}}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{\text{RAS}}$, $\overline{\text{CAS}}$<br>$\overline{\text{WE}}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the command to be executed by the SDRAM. |
| DQS | Input/ Output | Pulse | Active High | Active on both edges for data input and output.<br>Center aligned to input data<br>Edge aligned to output data |
| $A_0$ - $A_{13}$ | Input | Level | — | During a Bank Activate command cycle, $A_0$-$A_{13}$ defines the row address ($RA_0$-$RA_{13}$) when sampled at the rising clock edge.<br>During a Read or Write command cycle, $A_0$-$A_n$ defines the column address ($CA_0$-$CA_n$) when sampled at the rising clock edge.CAn depends on the SDRAM organization:<br><br>64M x 16 DDR $CA_n = CA_9$<br><br>In addition to the column address, $A_{10}$(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If $A_{10}$ is high, autoprecharge is selected and $BA_0$, $BA_1$ defines the bank to be precharged. If $A_{10}$ is low, autoprecharge is disabled.<br>During a Precharge command cycle, $A_{10}$(=AP) is used in conjunction with $BA_0$ and $BA_1$ to control which bank(s) to precharge. If $A_{10}$ is high, all four banks will be precharged simultaneously regardless of state of $BA_0$ and $BA_1$. |
| $BA_0$,<br>$BA_1$ | Input | Level | — | Selects which bank is to be active. |
| DQx | Input/ Output | Level | — | Data Input/Output pins operate in the same manner as on conventional DRAMs. |
| DM,<br>LDM,<br>UDM | Input | Pulse | Active High | In Write mode, DM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if is high for x 16 LDM corresponds to data on $DQ_0$-$DQ_7$, UDM corresponds to data on $DQ_8$-$DQ_{15}$. |
| $V_{DD}$, $V_{SS}$ | Supply | | | Power and ground for the input buffers and the core logic. |
| $V_{DDQ}$<br>$V_{SSQ}$ | Supply | — | — | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| $V_{REF}$ | Input | Level | — | SSTL Reference Voltage for Inputs |

## *Functional Description*

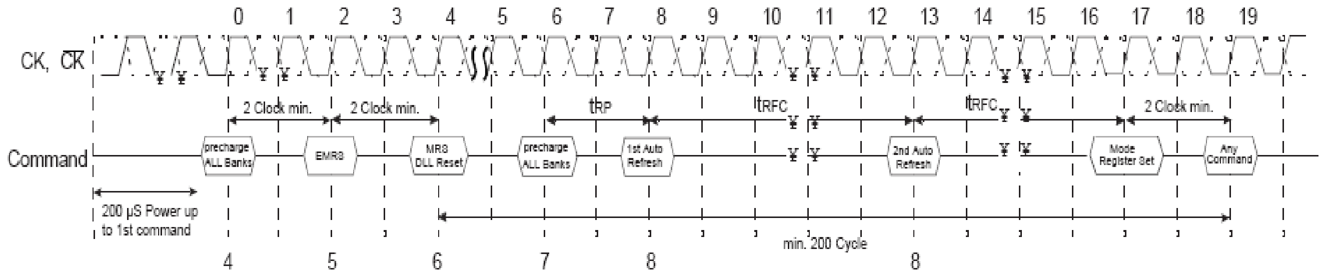
- Power-Up Sequence

  The following sequence is required for POWER UP.

  1. Apply power and attempt to maintain CKE at a low state (all other inputs may be undefined.)
     - Apply $V_{DD}$ before or at the same time as $V_{DDQ}$.
     - Apply $V_{DDQ}$ before or at the same time as $V_{TT}$ & Vref.
  2. Start clock and maintain stable condition for a minimum of 200us.
  3. The minimum of 200us after stable power and clock (CLK, $\overline{\text{CLK}}$), apply NOP & take CKE high.
  4. Precharge all banks.
  5. Issue EMRS to enable DLL.(To issue "DLL Enable" command, provide "Low" to $A_0$, "High" to $BA_0$ and "Low" to all of the rest address pins, $A_1$~$A_{13}$ and $BA_1$)
  6. Issue a mode register set command for "DLL reset". The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide "High" to $A_8$ and "Low" to $BA_0$)
  7. Issue precharge commands for all banks of the device.
  8. Issue 2 or more auto-refresh commands.
  9. Issue a mode register set command to initialize device operation.

Note1 Every "DLL enable" command resets DLL. Therefore sequence 6 can be skipped during power up. Instead of it, the additional 200 cycles of clock input is required to lock the DLL after enabling DLL.

**Power up Sequence & Auto Refresh(CBR)**



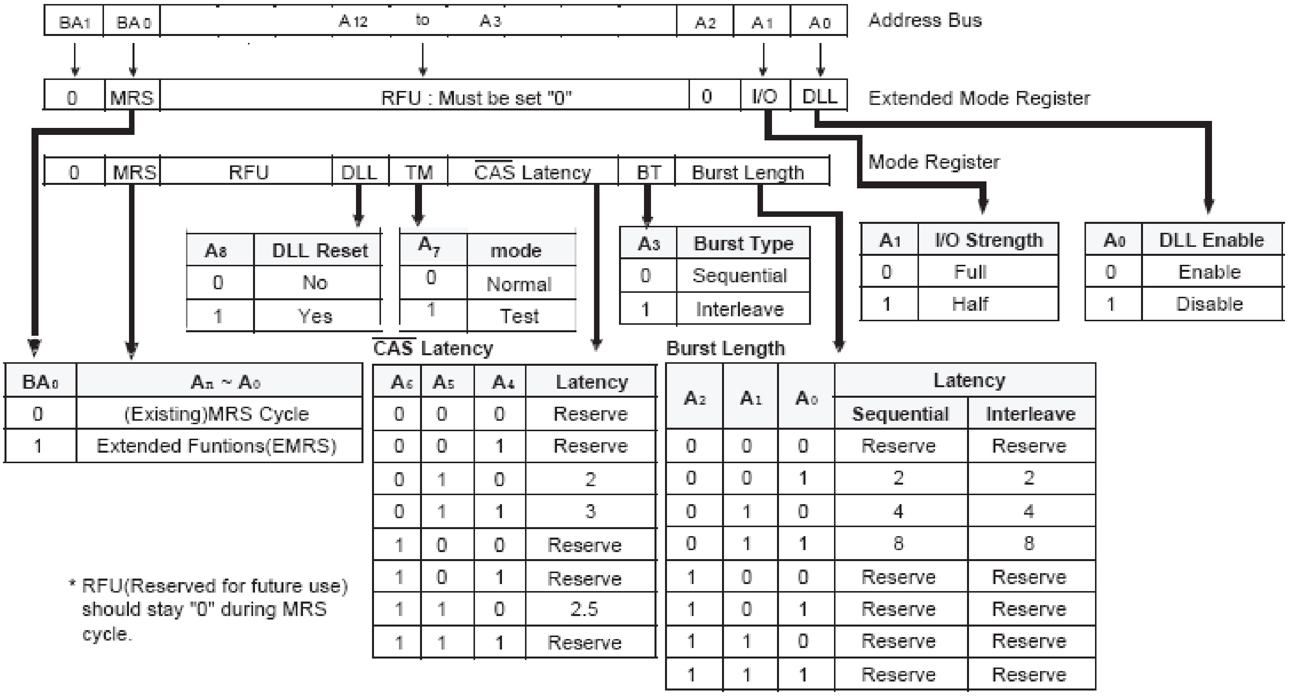
### *Extended Mode Register Set (EMRS)*

The extended mode register stores the data for enabling or disabling DLL. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on $BA_0$ (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins $A_0$ ~ $A_{12}$ and $BA_1$ in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. $A_0$ is used for DLL enable or disable. “High” on $BA_0$ is used for EMRS. All the other address pins except $A_0$ and $BA_0$ must be set to low for proper EMRS operation. $A_1$ is used at EMRS to indicate I/O strength $A_1$ = 0 full strength, $A_1$ = 1 half strength. Refer to the table for specific codes.

### *Mode Register Set (MRS)*

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for a variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $BA_0$ (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register). The state of address pins $A_0$ ~ $A_{12}$ in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and BA0 low is written in the mode register. Two clock cycles are required to meet $t_{MRD}$ spec. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses $A_0$ ~ $A_2$, addressing mode uses $A_3$, $\overline{CAS}$ latency (read latency from column address) uses $A_4$ ~ $A_6$. $A_7$ is a Alliance Memory specific test mode during production test. $A_8$ is used for DLL reset. $A_7$ must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.

1. MRS can be issued only at all banks precharge state.
2. Minimum tRP is required to issue MRS command.



| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| $A_7$ | mode |
|---|---|
| 0 | Normal |
| 1 | Test |

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A1 | I/O Strength |
|---|---|
| 0 | Full |
| 1 | Half |

| A0 | DLL Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| BA0 | An ~ A0 |
|---|---|
| 0 | (Existing)MRS Cycle |
| 1 | Extended Funtions(EMRS) |

$\overline{CAS}$ Latency

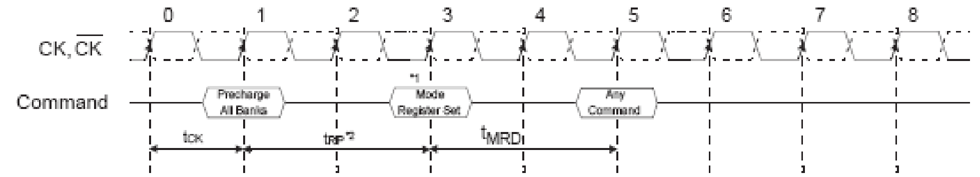
| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserve |
| 0 | 0 | 1 | Reserve |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserve |
| 1 | 0 | 1 | Reserve |
| 1 | 1 | 0 | 2.5 |
| 1 | 1 | 1 | Reserve |

Burst Length

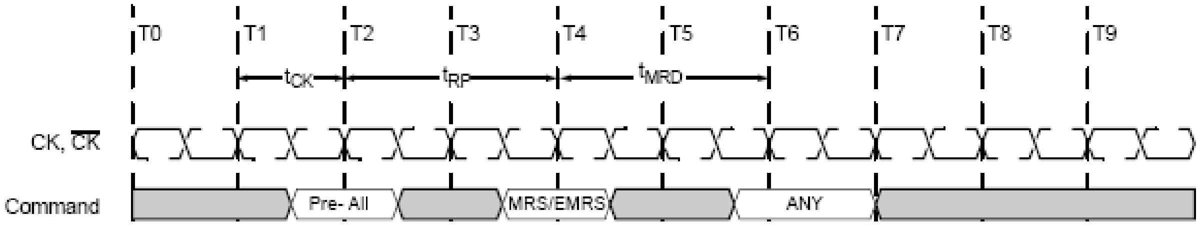
| A2 | A1 | A0 | Latency | |
|---|---|---|---|---|
| | | | Sequential | Interleave |
| 0 | 0 | 0 | Reserve | Reserve |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserve | Reserve |
| 1 | 0 | 1 | Reserve | Reserve |
| 1 | 1 | 0 | Reserve | Reserve |
| 1 | 1 | 1 | Reserve | Reserve |

* RFU(Reserved for future use) should stay "0" during MRS cycle.

**Mode Register Set**



## Mode Register Set Timing



Mode Register set (MRS) or Extended Mode Register Set (EMRS) can be issued only when all banks are in the idle state.

If a MRS command is issued to reset the DLL, then an additional 200 clocks must occur prior to issuing any new command to allow time for the DLL to lock onto the clock.

### Burst Mode Operation

Burst Mode Operation is used to provide a constant flow of data to memory locations (Write cycle), or from memory locations (Read cycle). Two parameters define how the burst mode will operate: burst sequence and burst length. These parameters are programmable and are determined by address bits $A_0$—$A_3$ during the Mode Register Set command. Burst type defines the sequence in which the burst data will be delivered or stored to the SDRAM. Two types of burst sequence are supported: sequential and interleave. The burst length controls the number of bits that will be output after a Read command, or the number of bits to be input after a Write command. The burst length can be programmed to values of 2, 4, or 8. See the Burst Length and Sequence table below for programming information.

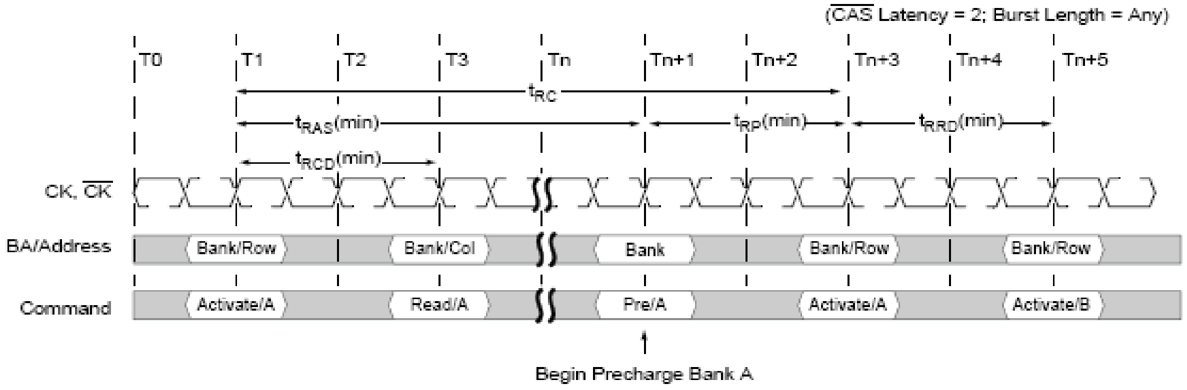
### Burst Length and Sequence

| Burst Length | Starting Length ($A_2$, $A_1$, $A_0$) | Sequential Mode | Interleave Mode |
|---|---|---|---|
| 2 | xx0 | 0, 1 | 0, 1 |
| | xx1 | 1, 0 | 1, 0 |
| 4 | x00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 000 | 0,1, 2, 3, 4, 5, 6, 7 | 0,1, 2, 3, 4, 5, 6, 7 |
| | 001 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 010 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 011 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 100 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 101 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 110 | 6, 7, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 111 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |

### Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SDRAM has four independent banks, so two Bank Select addresses ($BA_0$ and $BA_1$) are supported. The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from the Bank Activate command to the first Read or Write command must meet or exceed the minimum $\overline{RAS}$ to $\overline{CAS}$ delay time ($t_{RCD}$ min). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time ($t_{RRD}$ min).

**Bank Activation Timing**



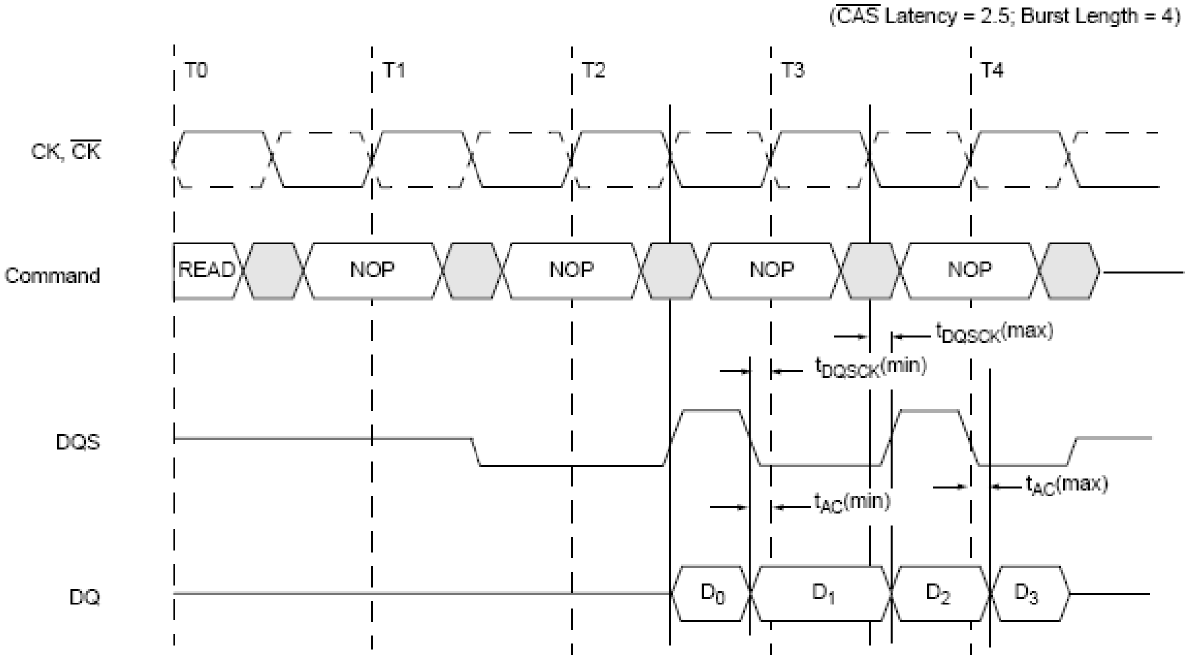
### Read Operation

With the DLL enabled, all devices operating at the same frequency within a system are ensured to have the same timing relationship between DQ and DQS relative to the CK input regardless of device density, process variation, or technology generation.

The data strobe signal (DQS) is driven off chip simultaneously with the output data (DQ) during each read cycle. The same internal clock phase is used to drive both the output data and data strobe signal off chip to minimize skew between data strobe and output data. This internal clock phase is nominally aligned to the input differential clock (CK, $\overline{CK}$) by the on-chip DLL. Therefore, when the DLL is enabled and the clock frequency is within the specified range for proper DLL operation, the data strobe (DQS), output data (DQ), and the system clock (CK) are all nominally aligned.

Since the data strobe and output data are tightly coupled in the system, the data strobe signal may be delayed and used to latch the output data into the receiving device. The tolerance for skew between DQS and DQ ($t_{DQSQ}$) is tighter than that possible for CK to DQ ($t_{AC}$) or DQS to CK ($t_{DQSCK}$).

## *Output Data (DQ) and Data Strobe (DQS) Timing Relative to the Clock (CK) During Read Cycles*



The minimum time during which the output data (DQ) is valid is critical for the receiving device (i.e., a memory controller device). This also applies to the data strobe during the read cycle since it is tightly coupled to the output data. The minimum data output valid time ($t_{DV}$) and minimum data strobe valid time ($t_{DQSV}$) are derived from the minimum clock high/low time minus a margin for variation in data access and hold time due to DLL jitter and power supply noise.

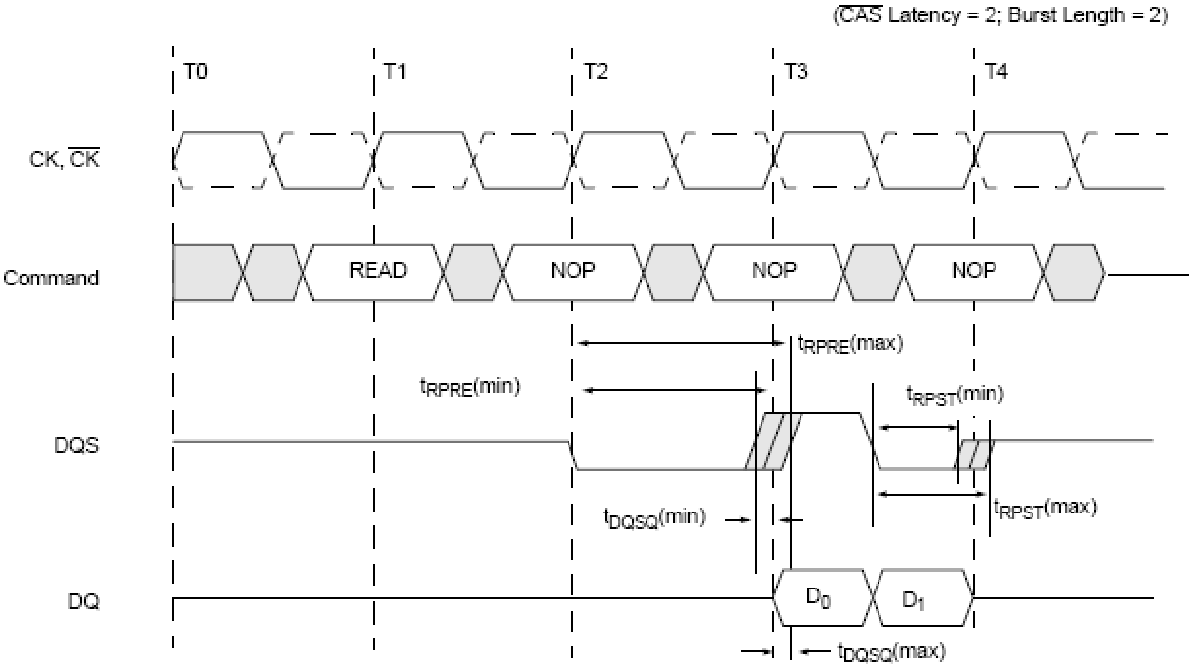
### *Read Preamble and Postamble Operation*

Prior to a burst of read data and given that the controller is not currently in burst read mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. The is referred to as the data strobe "read preamble" ($t_{RPRE}$). This transition from Hi-Z to logic low nominally happens one clock cycle prior to the first edge of valid data.

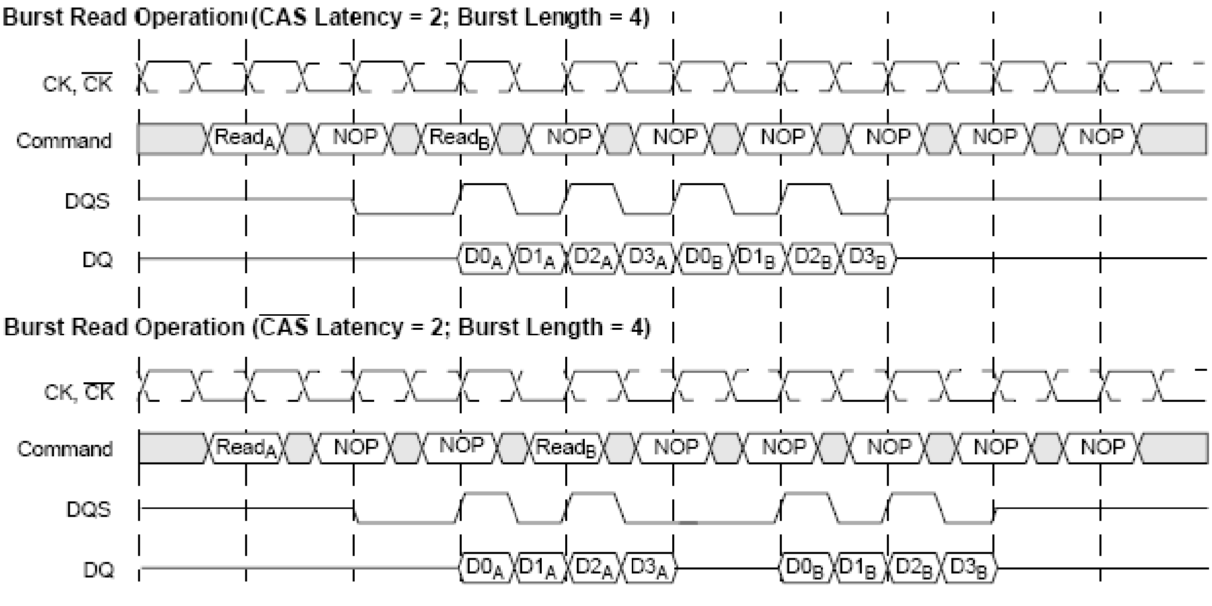
Once the burst of read data is concluded and given that no subsequent burst read operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe "read postamble" ($t_{RPST}$). This transition happens nominally one-half clock period after the last edge of valid data.

Consecutive or "gapless" burst read operations are possible from the same DDR SDRAM device with no requirement for a data strobe "read" preamble or postamble in between the groups of burst data. The data strobe read preamble is required before the DDR device drives the first output data off chip. Similarly, the data strobe postamble is initiated when the device stops driving DQ data at the termination of read burst cycles.

## Data Strobe Preamble and Postamble Timings for DDR Read Cycles



## Consecutive Burst Read Operation and Effects on the Data Strobe Preamble and Postamble



## *Precharge Operation*

The Precharge command is used to deactivate the open row in a particular bank or the open row in all banks. The bank (s) will be available for a subsequent row access a specified time ($t_{RP}$) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input $A_{10}$ determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs $BA_0$, $BA_1$ select the bank. Otherwise $BA_0$, $BA_1$ are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A Precharge command will be treated as NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

## *Auto Precharge Operation*

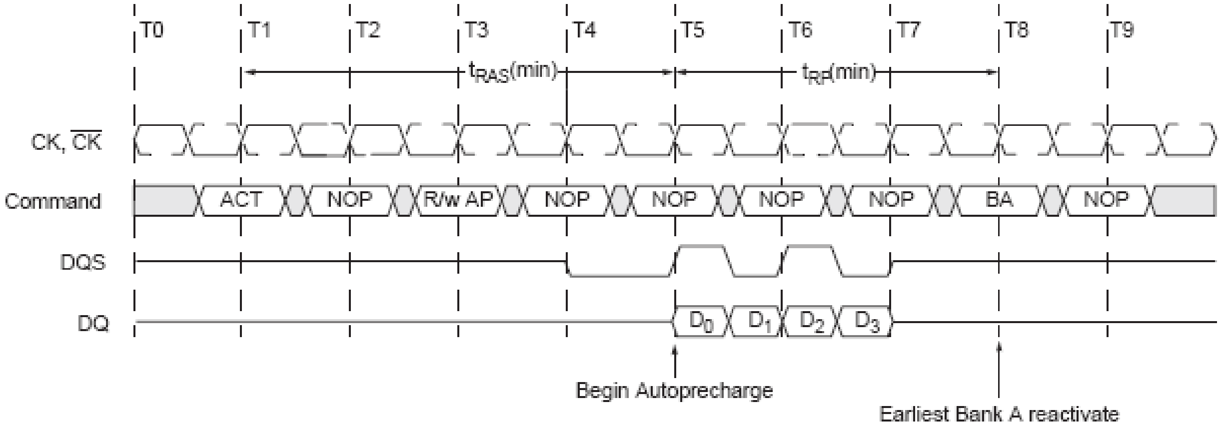
The Auto Precharge operation can be issued by having column address $A_{10}$ high when a Read or Write command is issued. If $A_{10}$ is low when a Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle once $t_{RAS}$(min) is satisfied. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

### Read with Auto Precharge

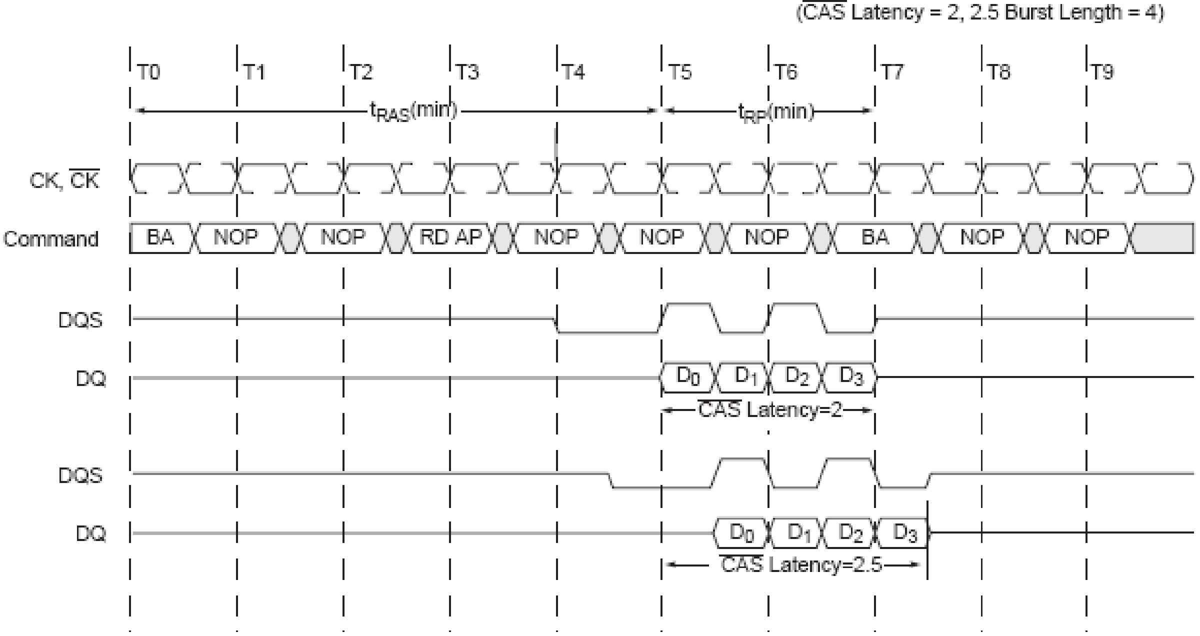
If a Read with Auto Precharge command is initiated, the DDR SDRAM will enter the precharge operation N-clock cycles measured from the last data of the burst read cycle where N is equal to the $\overline{CAS}$ latency programmed into the device. Once the autoprecharge operation has begun, the bank cannot be reactivated until the minimum precharge time ($t_{RP}$) has been satisfied.

***Read with Autoprecharge Timing***

($\overline{CAS}$ Latency = 2; Burst Length = 4)



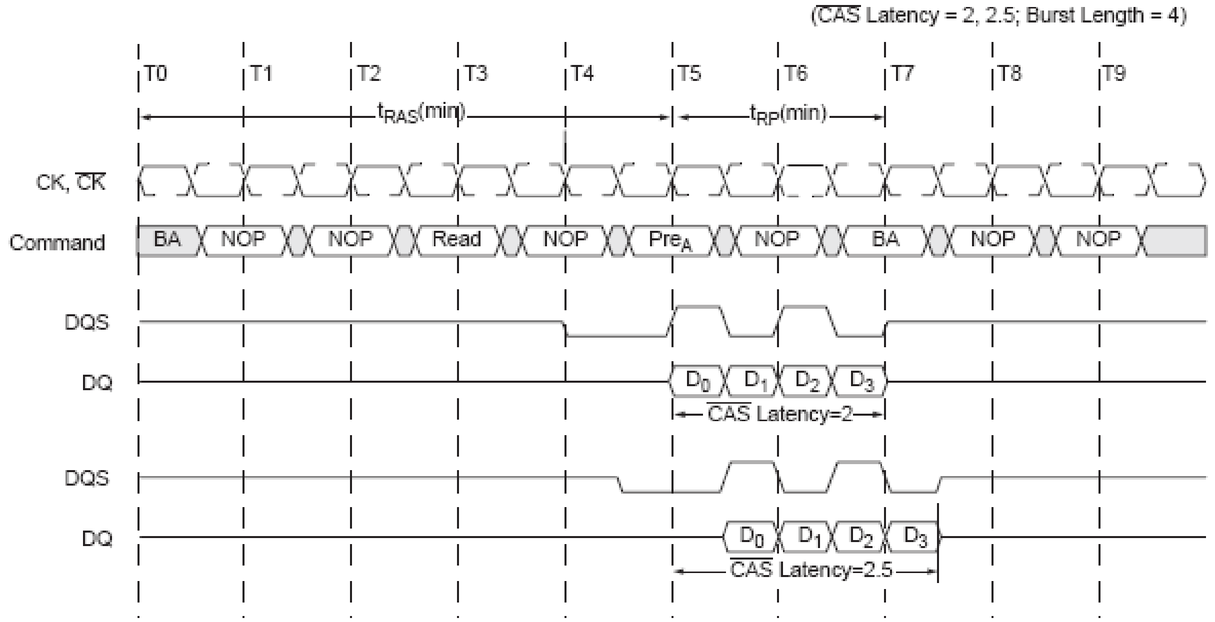
### Read with Autoprecharge Timing as a Function of $\overline{CAS}$ Latency



### Precharge Timing During Read Operation

For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be issued on the rising clock edge which is CAS latency (CL) clock cycles before the end of the Read burst. A new Bank Activate (BA) command may be issued to the same bank after the RAS precharge time ($t_{RP}$). A Precharge command can not be issued until $t_{RAS}$(min) is satisfied.

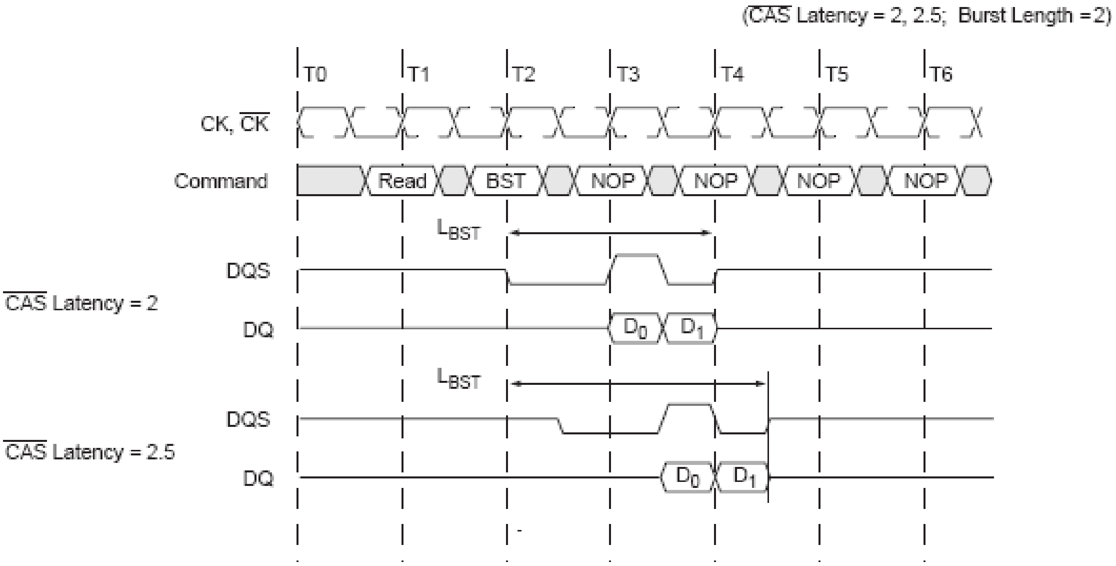
***Read with Precharge Timing as a Function of $\overline{CAS}$ Latency***



### Burst Stop Command

The Burst Stop command is valid only during burst read cycles and is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. When the Burst Stop command is issued during a burst Read cycle, both the output data (DQ) and data strobe (DQS) go to a high impedance state after a delay ($L_{BST}$) equal to the $\overline{CAS}$ latency programmed into the device. If the Burst Stop command is issued during a burst Write cycle, the command will be treated as a NOP command.

**Read Terminated by Burst Stop Command Timing**

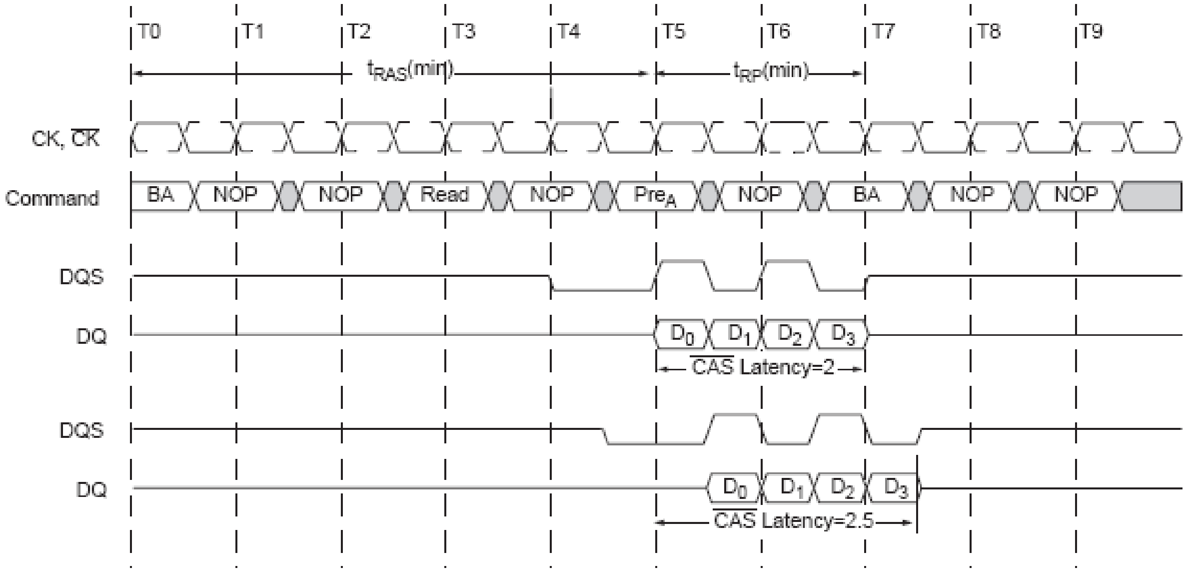


### Read Interrupted by a Precharge

A Burst Read operation can be interrupted by a precharge of the same bank. The Precharge command to Output Disable latency is equivalent to the $\overline{CAS}$ latency.

### *Read Interrupted by a Precharge Timing*

($\overline{CAS}$ Latency = 2, 2.5; Burst Length = 4)



### *Burst Write Operation*

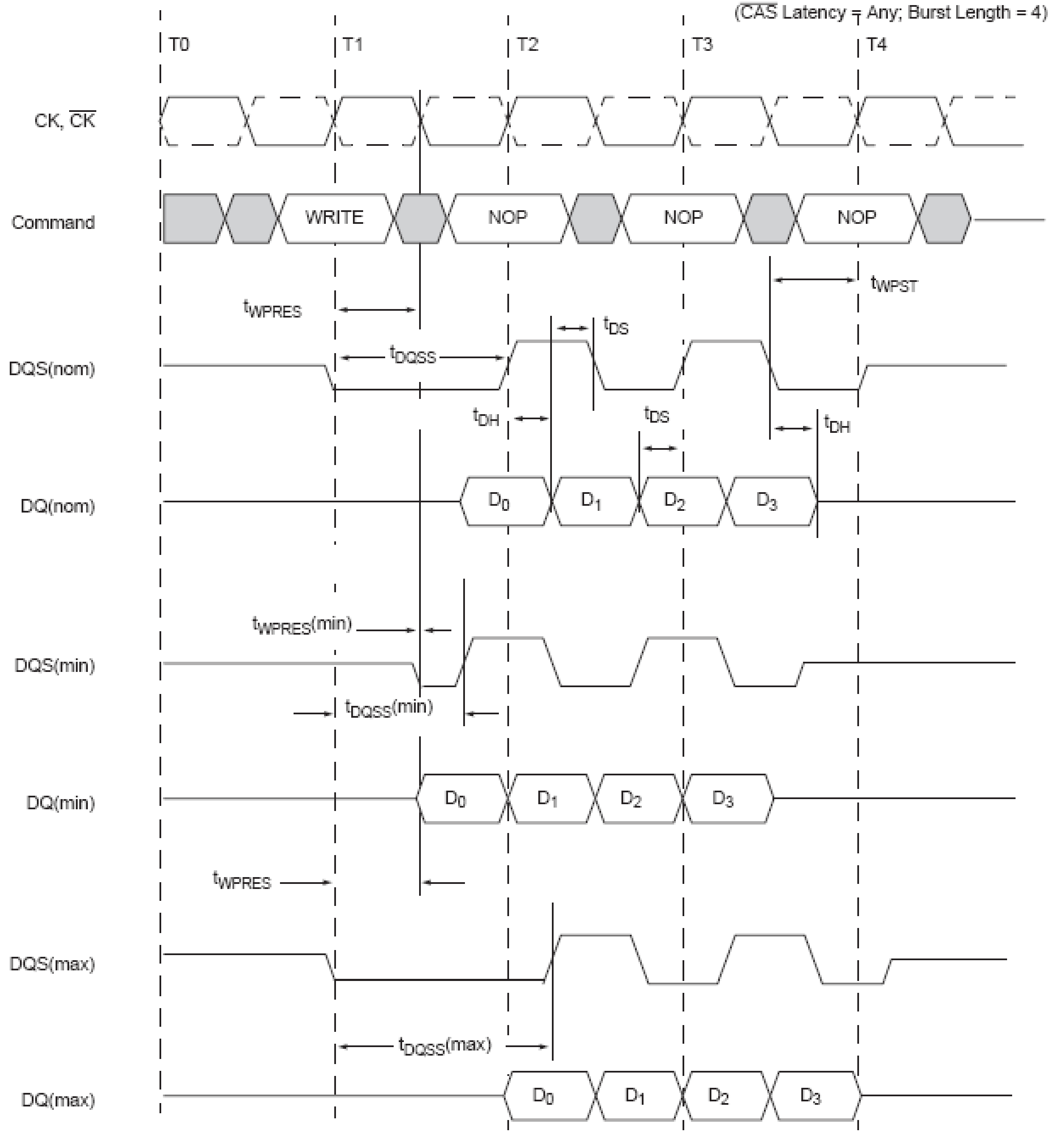
The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. The memory controller is required to provide an input data strobe (DQS) to the DDR SDRAM to strobe or latch the input data (DQ) and data mask (DM) into the device. During Write cycles, the data strobe applied to the DDR SDRAM is required to be nominally centered within the data (DQ) and data mask (DM) valid windows. The data strobe must be driven high nominally one clock after the write command has been registered. Timing parameters $t_{DQSS}$(min) and $t_{DQSS}$(max) define the allowable window when the data strobe must be driven high.

Input data for the first Burst Write cycle must be applied one clock cycle after the Write command is registered into the device (WL=1). The input data valid window is nominally centered around the midpoint of the data strobe signal. The data window is defined by DQ to DQS setup time ($t_{QDQSS}$) and DQ to DQS hold time ($t_{QDQSH}$). All data inputs must be supplied on each rising and falling edge of the data strobe until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

### Write Preamble and Postamble Operation

Prior to a burst of write data and given that the controller is not currently in burst write mode, the data strobe signal (DQS), must transition from Hi-Z to a valid logic low. This is referred to as the data strobe "write preamble". This transition from Hi-Z to logic low nominally happens on the falling edge of the clock after the write command has been registered by the device. The preamble is explicitly defined by a setup time ($t_{WPRES}$(min)) and hold time ($t_{WPREH}$(min)) referenced to the first falling edge of CK after the write command.

## Burst Write Timing

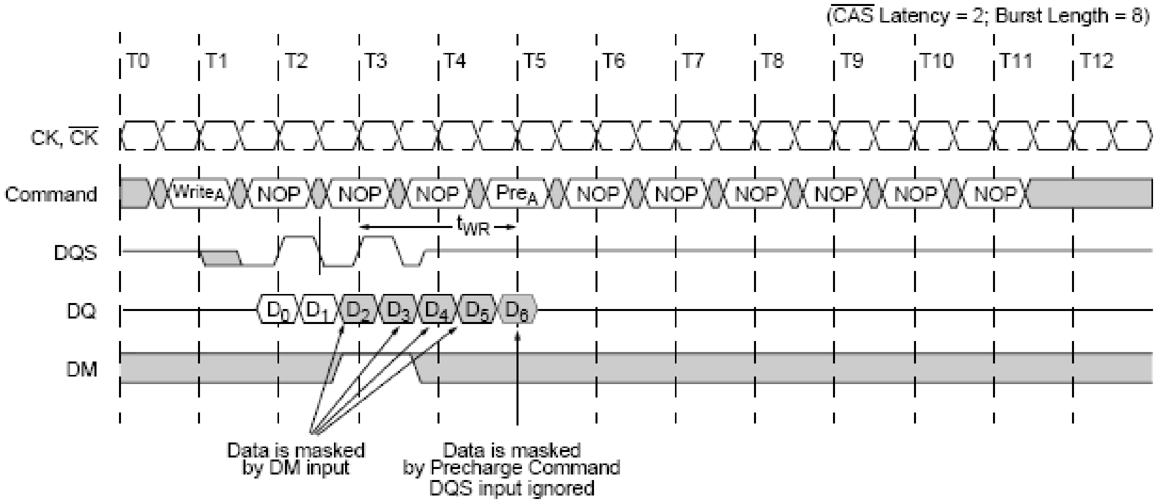


Once the burst of write data is concluded and given that no subsequent burst write operations are initiated, the data strobe signal (DQS) transitions from a logic low level back to Hi-Z. This is referred to as the data strobe “write postamble”. This transition happens nominally one-half clock period after the last data of the burst cycle is latched into the device.

### Write Interrupted by a Precharge

A Burst Write can be interrupted before completion of the burst by a Precharge command, with the only restriction being that the interval that separates the commands be at least one clock cycle.

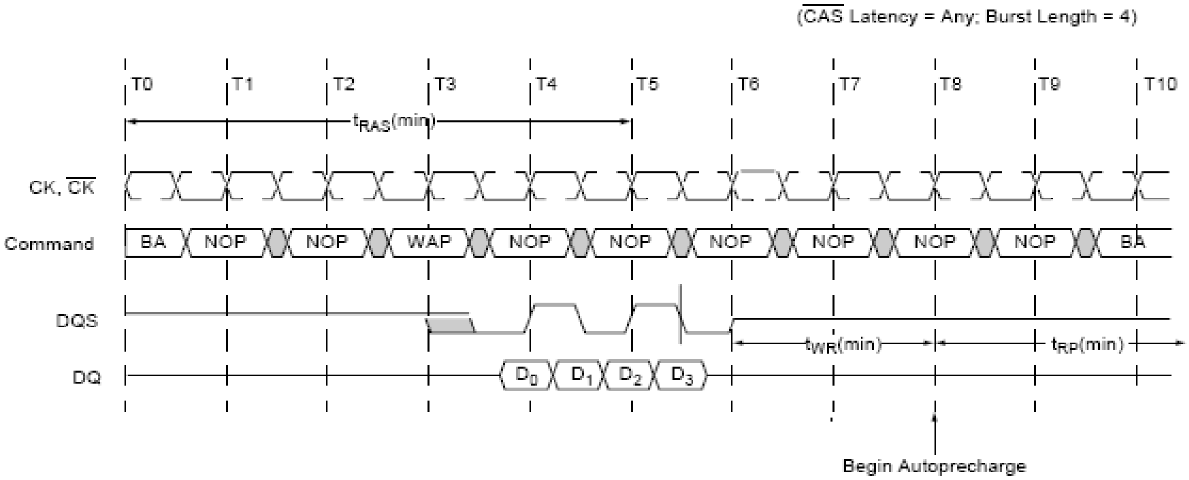
***Write Interrupted by a Precharge Timing***



### Write with Auto Precharge

If A10 is high when a Write command is issued, the Write with auto Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping $t_{WR}$ (min.).

***Write with Auto Precharge Timing***

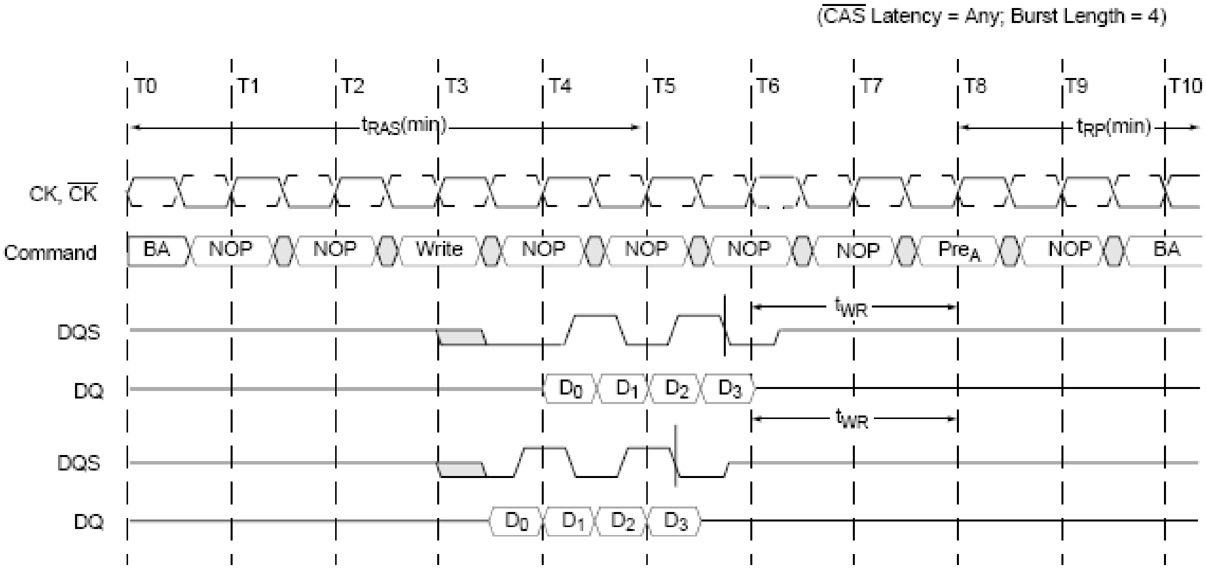


### *Precharge Timing During Write Operation*

Precharge timing for Write operations in DRAMs requires enough time to satisfy the write recovery requirement. This is the time required by a DRAM sense amp to fully store the voltage level. For DDR SDRAMs, a timing parameter ($t_{WR}$) is used to indicate the required amount of time between the last valid write operation and a Precharge command to the same bank.

The "write recovery" operation begins on the rising clock edge after the last DQS edge that is used to strobe in the last valid write data. "Write recovery" is complete on the next 2nd rising clock edge that is used to strobe in the Precharge command.

### *Write with Precharge Timing*



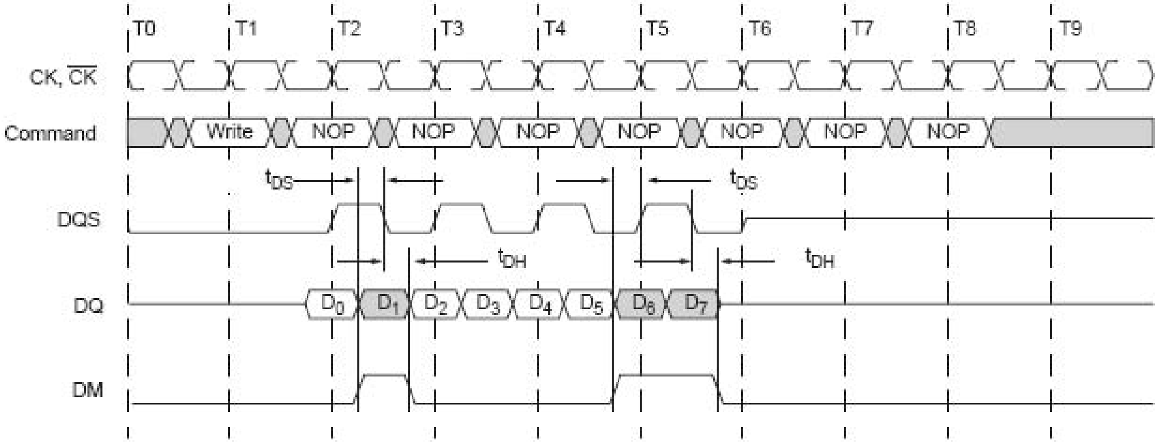
### *Data Mask Function*

The DDR SDRAM has a Data Mask function that is used in conjunction with the Write cycle, but not the Read cycle. When the Data Mask is activated (DM high) during a Write operation, the Write is blocked (Mask to Data Latency = 0).

When issued, the Data Mask must be referenced to both the rising and falling edges of Data Strobe.

***Data Mask Timing***

($\overline{CAS}$ Latency = Any; Burst Length = 8)



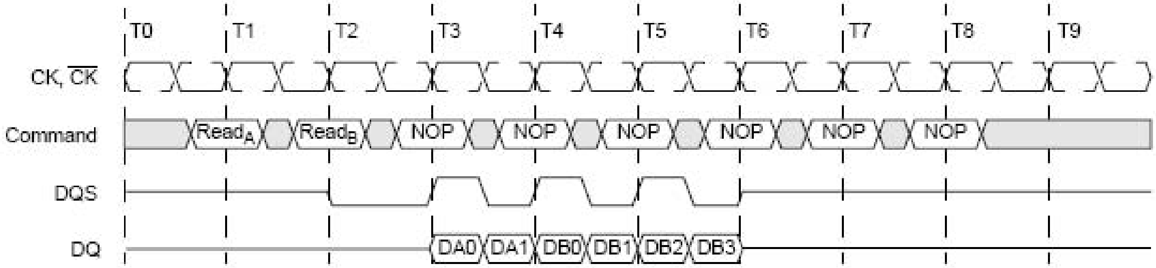
### *Burst Interruption*

#### Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by issuing a new Read command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears on the bus. Read commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Read with autoprecharge command with a Read command.

***Read Interrupted by a Read Command Timing***

($\overline{CAS}$ Latency = 2; Burst Length = 4)

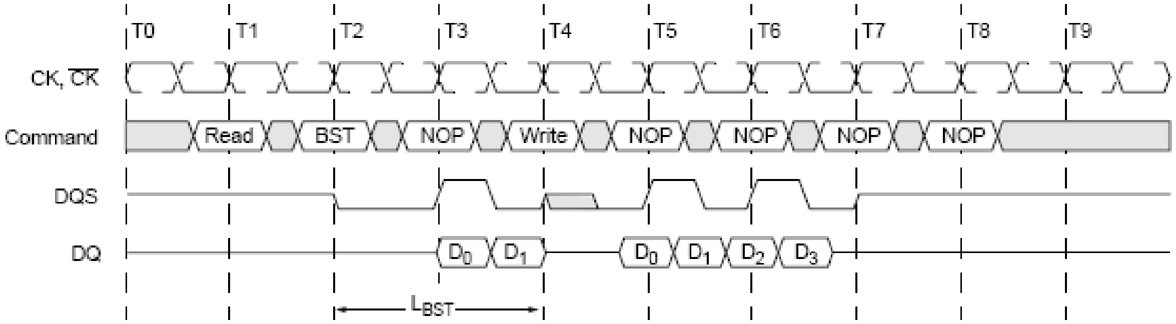


### Read Interrupted by a Write

To interrupt a Burst Read with a Write command, a Burst Stop command must be asserted to stop the burst read operation and 3-state the DQ bus. Additionally, control of the DQS bus must be turned around to allow the memory controller to drive the data strobe signal (DQS) into the DDR SDRAM for the write cycles. Once the Burst Stop command has been issued, a Write command can not be issued until a minimum delay or latency ($L_{BST}$) has been satisfied. This latency is measured from the Burst Stop command and is equivalent to the $\overline{CAS}$ latency programmed into the mode register. In instances where $\overline{CAS}$ latency is measured in half clock cycles, the minimum delay ($L_{BST}$) is rounded up to the next full clock cycle (i.e., if CL=2 then $L_{BST}$=2, if CL=2.5 then $L_{BST}$=3). It is illegal to interrupt a Read with autoprecharge command with a Write command.

*Read Interrupted by Burst Stop Command Followed by a Write Command Timing*

($\overline{CAS}$ Latency = 2; Burst Length = 4)

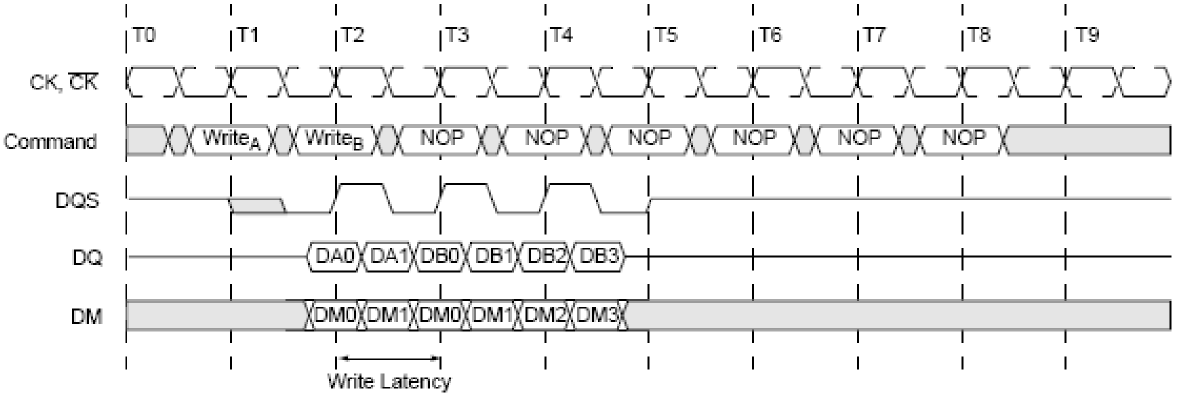


### Write Interrupted by a Write

A Burst Write can be interrupted before completion by a new Write command to any bank. When the previous burst is interrupted, the remaining addresses are overridden with a full burst length starting with the new address. The data from the first Write command continues to be input into the device until the Write Latency of the interrupting Write command is satisfied (WL=1) At this point, the data from the interrupting Write command is input into the device. Write commands can be issued on each rising edge of the system clock. It is illegal to interrupt a Write with autoprecharge command with a Write command.

*Write Interrupted by a Write Command Timing*

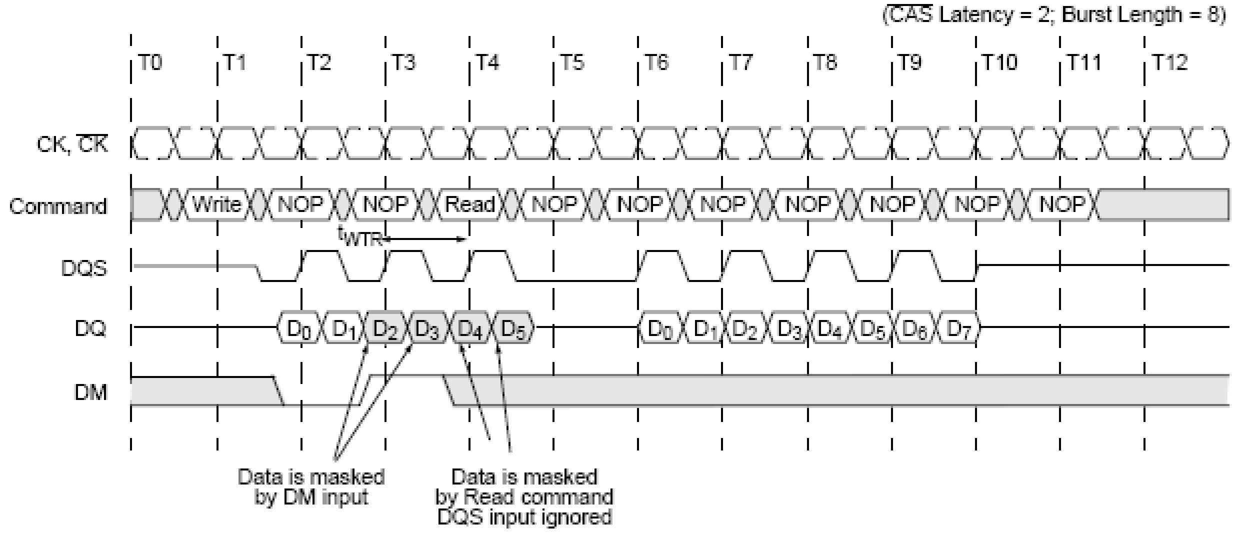
($\overline{CAS}$ Latency = Any; Burst Length = 4)



### Write Interrupted by a Read

A Burst Write can be interrupted by a Read command to any bank. If a burst write operation is interrupted prior to the end of the burst operation, then the last two pieces of input data prior to the Read command must be masked off with the data mask (DM) input pin to prevent invalid data from being written into the memory array. Any data that is present on the DQ pins coincident with or following the Read command will be masked off by the Read command and will not be written to the array. The memory controller must give up control of both the DQ bus and the DQS bus at least one clock cycle before the read data appears on the outputs in order to avoid contention. In order to avoid data contention within the device, a delay is required ($t_{WTR}$) from the first positive CK edge after the last desired data in the pair $t_{WTR}$ before a Read command can be issued to the device. It is illegal to interrupt a Write with autoprecharge command with a Read command.

*Write Interrupted by a Read Command Timing*



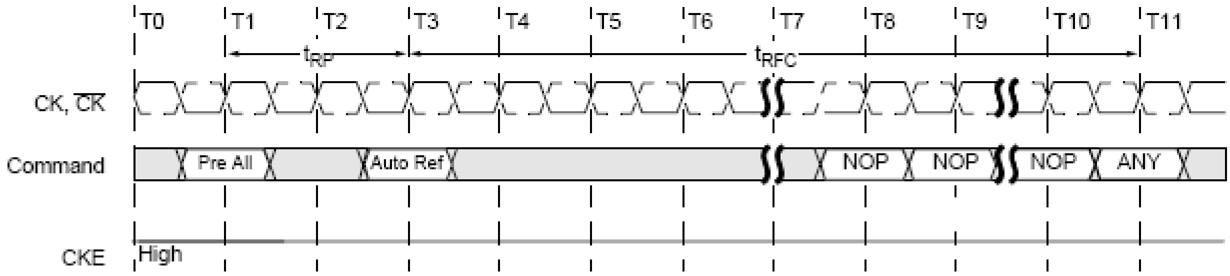
Data is masked by DM input

Data is masked by Read command DQS input ignored

## *Auto Refresh*

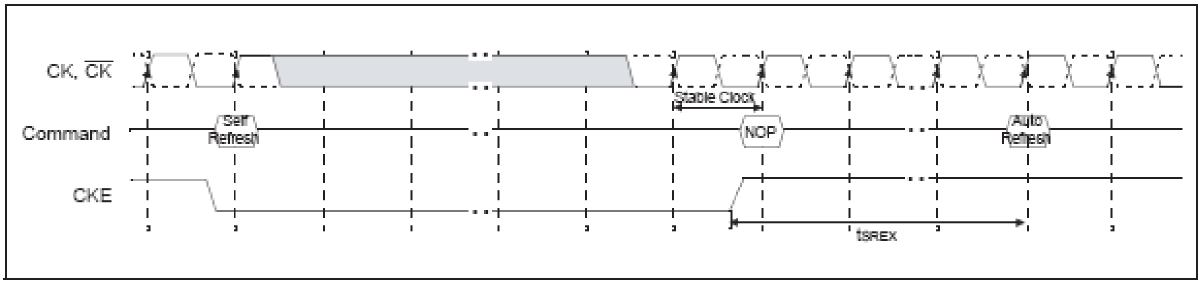
The Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock. All banks must be precharged and idle for a $t_{RP}$(min) before the Auto Refresh command is applied. No control of the address pins is required once this cycle has started because of the internal address counter. When the Auto Refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate command or subsequent Auto Refresh command must be greater than or equal to the $t_{RFC}$(min). Commands may not be issued to the device once an Auto Refresh cycle has begun. $\overline{CS}$ input must remain high during the refresh period or NOP commands must be registered on each rising edge of the CK input until the refresh period is satisfied.

*Auto Refresh Timing*



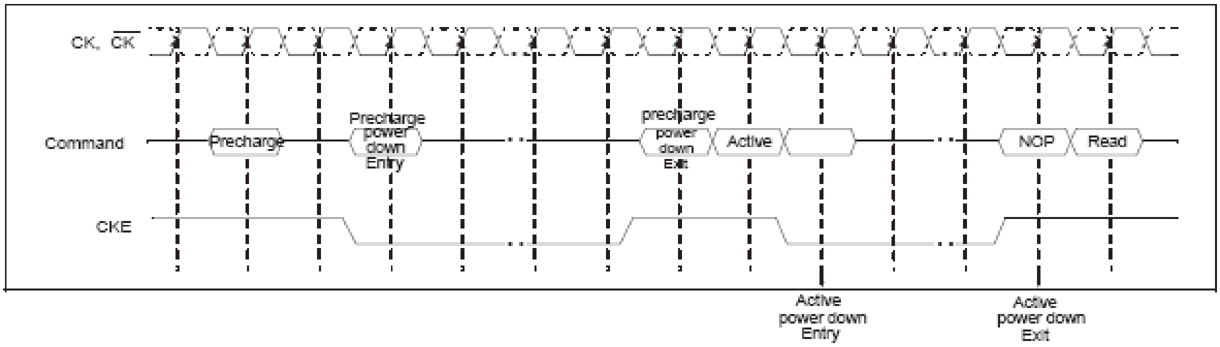
## Self Refresh

A self refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock (CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than $t_{SREX}$ for locking of DLL. The auto refresh is required before self refresh entry and after self refresh exit.



## Power Down Mode

The power down mode is entered when CKE is low and exited when CKE is high. Once the power down mode is initiated, all of the receiver circuits except clock, CKE and DLL circuit are gated off to reduce power consumption. All banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1tck+tIS prior to row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period ($t_{REF}$) of the device.



## *TRUTH TABLE – CKE*

| CKEn-1 | CKEn | CURRENT STATE | COMMANDn | ACTIONn | NOTES |
|---|---|---|---|---|---|
| L | L | Power-Down | X | Maintain Power-Down | |
| | | Self Refresh | X | Maintain Self Refresh | |
| | | | | | |
| L | H | Power-Down | DESELECT or NOP | Exit Power-Down | |
| | | Self Refresh | DESELECT or NOP | Exit Self Refresh | 5 |
| | | | | | |
| H | L | All Banks Idle | DESELECT or NOP | Precharge Power-Down Entry | |
| | | Bank(s) Active | DESELECT or NOP | Active Power-Down Entry | |
| | | All Banks Idle | AUTO REFRESH | Self Refresh Entry | |
| H | H | | See Truth Table 3 | | |

**NOTE:**

1. $CKE_n$ is the logic state of CKE at clock edge *n*; $CKE_{n-1}$ was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n*, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the $^{t}XSR$ period.
   A minimum of 200 clock cycles is needed before applying a read command, for the DLL to lock.

### DDR SDRAM SIMPLIFIED COMMAND TRUTH TABLE

| Command | | CKEn-1 | CKEn | CS | RAS | CAS | WE | ADDR | A10/ AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Extended Mode Register Set | | H | X | L | L | L | L | OP code | | | 1,2 |
| Device Deselect | | H | X | H | X | X | X | X | | | 1 |
| No Operation | | | | L | H | H | H | | | | |
| Bank Active | | H | X | L | L | H | H | RA | | V | 1 |
| Read | | H | X | L | H | L | H | CA | L | V | 1 |
| Read with Autoprecharge | | | | | | | | | H | | 1,3 |
| Write | | H | X | L | H | L | L | CA | L | V | 1 |
| Write with Autoprecharge | | | | | | | | | H | | 1,4 |
| Precharge All Banks | | H | X | L | L | H | L | X | H | X | 1,5 |
| Precharge selected Bank | | | | | | | | | L | V | 1 |
| Read Burst Stop | | H | X | L | H | H | L | X | | | 1 |
| Auto Refresh | | H | H | L | L | L | H | X | | | 1 |
| Self Refresh | Entry | H | L | L | L | L | H | X | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | |
| Precharge Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| | Exit | L | H | H | X | X | X | | | | 1 |
| | | | | L | H | H | H | | | | 1 |
| Active Power Down Mode | Entry | H | L | H | X | X | X | X | | | 1 |
| | | | | L | V | V | V | | | | 1 |
| | Exit | L | H | X | | | | | | | 1 |

( H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation )

**Note :**

1. LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of $A_0$~$A_{12}$ and $BA_0$~$BA_1$ used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If $A_{10}$/AP is High when Precharge command being issued, $BA_0$/$BA_1$ are ignored and all banks are selected to be precharged.

### *TRUTH TABLE – Current State Bank n - Command to Bank n*

| CURRENT STATE | /CS | /RAS | /CAS | /WE | COMMAND/ACTION | NOTES |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | DESELECT (NOP/continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/continue previous operation) | |
| Idle | L | L | H | H | ACTIVE (select and activate row) | |
| | L | L | L | H | AUTO REFRESH | 7 |
| | L | L | L | L | MODE REGISTER SET | 7 |
| Row Active | L | H | L | H | READ (select column and start READ burst) | 10 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (deactivate row in bank or banks) | 8 |
| Read (Auto Precharge Disabled) | L | H | L | H | READ (select column and start new READ burst) | 10 |
| | L | L | H | L | PRECHARGE (truncate READ burst, start PRECHARGE) | 8 |
| | L | H | H | L | BURST TERMINATE | 9 |
| Write (Auto Precharge Disabled) | L | H | L | H | READ (select column and start READ burst) | 10, 11 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (truncate WRITE burst, start PRECHARGE) | 8, 11 |

**NOTE:**

1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH (see Truth Table 2) and after $^tXSR$ has been met (if the previous state was self refresh).

2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.

3. Current state definitions:

Idle: The bank has been precharged, and $^tRP$ has been met.

Row Active: A row in the bank has been activated, and $^tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

Precharging: Starts with registration of a PRECHARGE command and ends when $^tRP$ is met. Once $^tRP$ is met, the bank will be in the idle state.

**NOTE: (continued)**

Row Activating: Starts with registration of an ACTIVE command and ends when $^t$RCD is met. Once $^t$RCD is met, the bank will be in the "row active" state.

Read w/Auto-Precharge Enabled: Starts with registration of a READ command with AUTO PRECHARGE enabled and ends when $^t$RP has been met. Once $^t$RP is met, the bank will be in the idle state.

Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when $^t$RP has been met. Once $^t$RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

Refreshing: Starts with registration of an AUTO REFRESH command and ends when $^t$RC is met. Once $^t$RFC is met, the DDR SDRAM will be in the "all banks idle" state.

Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when $^t$MRD has been met. Once $^t$MRD is met, the DDR SDRAM will be in the "all banks idle" state.

Precharging All: Starts with registration of a PRECHARGE ALL command and ends when $^t$RP is met. Once $^t$RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.
11. Requires appropriate DM masking

### *TRUTH TABLE – Current State Bank n - Command to Bank m*

| CURRENT STATE | /CS | /RAS | /CAS | /WE | COMMAND/ACTION | NOTES |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | DESELECT (NOP/continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/continue previous operation) | |
| Idle | X | X | X | X | Any Command Otherwise Allowed to Bank m | |
| Row Activating, Active, or Precharging | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 7 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 7 |
| | L | L | H | L | PRECHARGE | |
| Read (Auto-Precharge Disabled) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start new READ burst) | 7 |
| | L | L | H | L | PRECHARGE | |
| Write (Auto- Precharge Disabled) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 7, 8 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 7 |
| | L | L | H | L | PRECHARGE | |
| Read (With Auto-Precharge) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start new READ burst) | 3a, 7 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 3a, 7, 9 |
| | L | L | H | L | PRECHARGE | |
| Write (With Auto-Precharge) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 3a, 7 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 3a, 7 |
| | L | L | H | L | PRECHARGE | |

**NOTE:**

1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH (see Truth Table 2) and after $^tXSR$ has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted, i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

Idle: The bank has been precharged, and $^tRP$ has been met.

Row Active: A row in the bank has been activated, and $^tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.

Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

Write: A WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

**NOTE: (continued)**

Read with Auto Precharge Enabled: See following text

Write with Auto Precharge Enabled: See following text

3a. The Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states can each be broken into two parts: the access period and the precharge period. For Read with Auto Precharge, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For Write with Auto Precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or $^{t}$RP) begins.

During the precharge period of the Read with Auto Precharge Enabled or Write with Auto Precharge Enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied; All other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).

3b. This device supports "concurrent auto precharge". This feature allows a read with auto precharge enabled, or a write with auto precharge enabled, to be followed by any command to the other banks, as long as that command does not interrrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided.)

3c. The minimum delay from a read or write command with auto precharge enable, to a command to a different bank, is sumarized below, for both cases of "concurrent auto precharge," supported or not:

| From Command | To Command (different bank) | Minimum Delay without Concurrent Auto Precharge Support | Minimum Delay with Concurrent Auto Precharge Support | Units |
|---|---|---|---|---|
| Write w/AP | Read or Read w/AP | 1+(BL/2)+(tWR/tCK) (rounded up) | 1+(BL/2)+tWTR | tCK |
| | Write or Write w/AP | 1+(BL/2)+(tWR/tCK) (rounded up) | BL/2 | tCK |
| | Precharge or Activate | 1 | | tCK |
| Read w/AP | Read or Read w/AP | BL/2 | | tCK |
| | Write or Write w/AP | CL(rounded up) + (BL/2) | | tCK |
| | Precharge or Activate | 1 | | tCK |

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.

5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

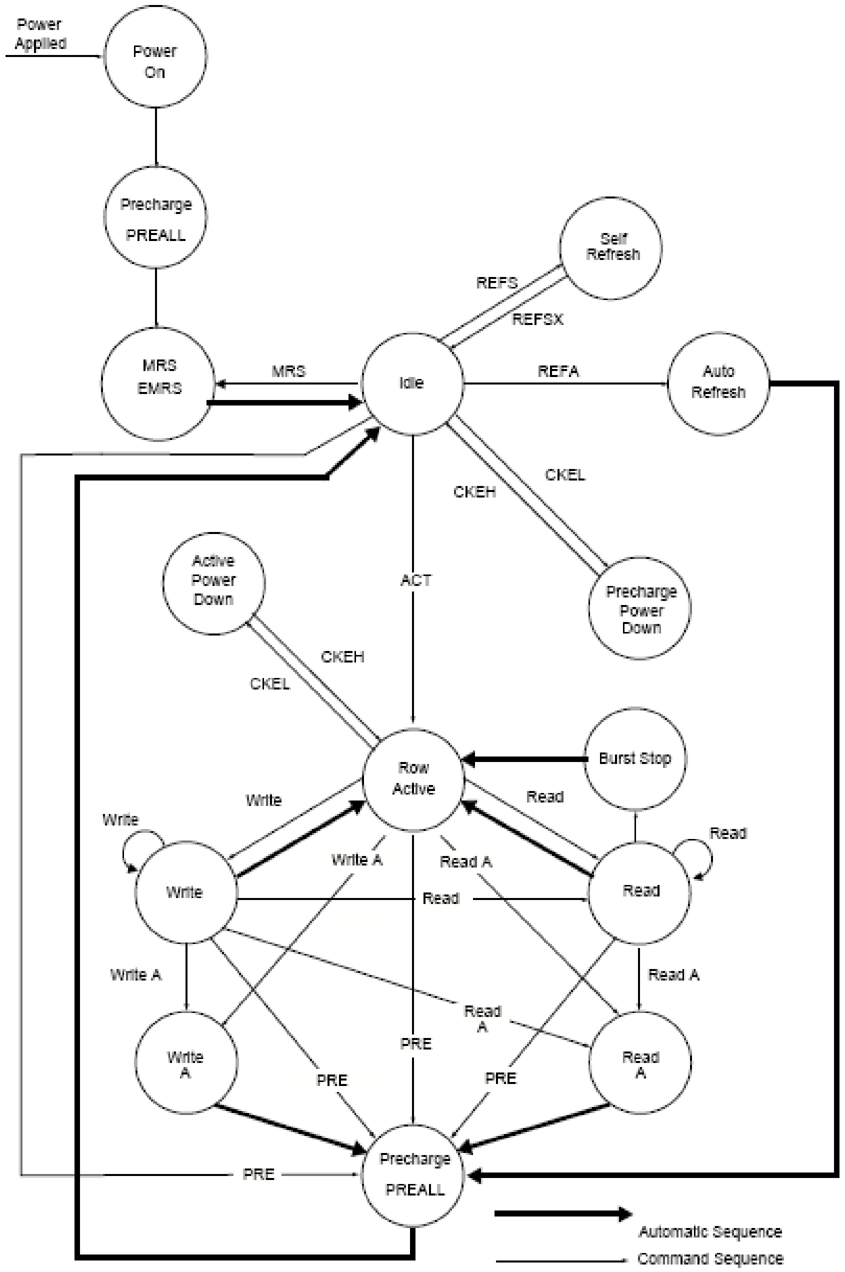
6. All states and sequences not shown are illegal or reserved.

7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with AUTO PRECHARGE enabled and READs or WRITEs with AUTO PRECHARGE disabled.

8. Requires appropriate DM masking.

9. A WRITE command may be applied after the completion of data output.

### Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

## *DC Operating Conditions & Specifications*

### DC Operating Conditions

Recommended operating conditions ( Voltage referenced to VSS = 0V )

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Supply voltage ( for device with a nominal $V_{DD}$ of 2.5V ) | $V_{DD}$ | 2.3 | 2.7 | | |
| Supply voltage ( $V_{DD}$ of 2.6V for DDR400 device ) | $V_{DD}$ | 2.5 | 2.7 | | |
| I/O Supply voltage | $V_{DDQ}$ | 2.3 | 2.7 | V | |
| I/O Supply voltage for DDR400 device | $V_{DDQ}$ | 2.5 | 2.7 | V | |
| I/O Reference voltage | $V_{REF}$ | 0.49*VDDQ | 0.51*VDDQ | V | 1 |
| I/O Termination voltage(system) | $V_{TT}$ | $V_{REF}$-0.04 | $V_{REF}$+0.04 | V | 2 |
| Input logic high voltage | $V_{IH}$(DC) | $V_{REF}$+0.15 | $V_{DDQ}$+0.3 | V | |
| Input logic low voltage | $V_{IL}$(DC) | -0.3 | $V_{REF}$-0.15 | V | |
| Input Voltage Level, CK and $\overline{CK}$ inputs | $V_{IN}$(DC) | -0.3 | $V_{DDQ}$+0.3 | V | |
| Input Differential Voltage, CK and $\overline{CK}$ inputs | $V_{ID}$(DC) | 0.3 | $V_{DDQ}$+0.6 | V | 3 |
| Input leakage current | $I_I$ | -2 | 2 | uA | |
| Output leakage current | $I_{OZ}$ | -5 | 5 | uA | |
| Output High Current ($V_{OUT}$ = 1.95V) | $I_{OH}$ | -16.8 | | mA | |
| Output Low Current ($V_{OUT}$ = 0.35V) | $I_{OL}$ | 16.8 | | mA | |

**Notes:** 1. $V_{REF}$ is expected to be equal to 0.5*$V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on $V_{REF}$ may not exceed 2% of the DC value

2. $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$, and must track variations in the DC level of $V_{REF}$

3. $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

## *IDD Max Specifications and Conditions*

( $V_{DDQ}$=2.5V± 0.2V, $V_{DD}$=2.5 ±0.2V, )

| Conditions | | Version | | |
|---|---|---|---|---|
| | | Symbol | -6 | Unit |
| **Operating current - One bank Active-Precharge;** tRC=tRCmin; tCK=tCKmin; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | | IDD0 | 85 | mA |
| **Operating current - One bank operation;** One bank open, BL=2 | | IDD1 | 105 | mA |
| **Precharge power-down standby current;** All banks idle; power - down mode; CKE = <VIL(max); tCK=tCKmin; Vin = Vref for DQ,DQS and DM | | IDD2P | 6 | mA |
| **Precharge Floating standby current;** CS# > =VIH(min); All banks idle; CKE > = VIH(min); tCK=tCKmin; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DQS and DM | | IDD2F | 30 | mA |
| **Precharge Quiet standby current;** CS# > = VIH(min); All banks idle; CKE > = VIH(min); tCK=tCKmin; Address and other control inputs stable with keeping >= VIH(min) or =<VIL(max); Vin = Vref for DQ, DQS and DM | | IDD2Q | 25 | mA |
| **Active power - down standby current;** one bank active; power-down mode; CKE=< VIL (max); tCK=tCKmin; Vin = Vref for DQ, DQS and DM | | IDD3P | 15 | mA |
| **Active standby current;** CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; tCK=tCKmin; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle | | IDD3N | 35 | mA |
| **Operating current - burst read;** Burst length = 2; reads; continuous burst; One bank active; address and control inputs changing once per clock cycle; tCK=tCKmin; 50% of data changing at every burst; Iout = 0 m A | | IDD4R | 115 | mA |
| **Operating current - burst write;** Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; tCK=tCKmin; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst | | IDD4W | 145 | mA |
| **Auto refresh current;** tRC = tRFCmin; tCK=tCKmin; burst refresh; address and control inputs changing once per clock cycle; data bus inputs are stable | tREFC=tRFC (MIN) | IDD5 | 185 | mA |
| | tREFC=7.8ms | IDD5A | 9 | mA |
| **Self-refresh current;** CKE =< 0.2V; External clock should be on; tCK=tCKmin. | | IDD6 | 3 | mA |
| **Operating current - Four bank operation;** Four bank interleaving with BL=4 | | IDD7 | 230 | mA |

## DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7

### IDD1: Operating current: One bank operation

1. Typical Case: VDD = 2.5V, T=25 °C for DDR266, 333; VDD = 2.6V , T=25 °C for DDR400, 500
2. Worst Case: VDD = 2.7V, T= 0 °C
3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA
4. Timing patterns

- DDR266 (133 Mhz, CL=2.5): tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
  Read: A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
  50% of data changing at every burst
- DDR333(166Mhz, CL=2.5): tCK = 6ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 10*tCK, tRAS = 7*tCK
  Read: A0 N N R0 N N N P0 N N A0 N - repeat the same timing with random address changing
  50% of data changing at every burst
- DDR400(200Mhz, CL=3): tCK = 5ns, CL=3, BL=4, tRCD = 3*tCK, tRC = 11*tCK, tRAS = 8*tCK
  Read: A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing
  50% of data changing at every burst
- DDR500(250Mhz, CL=3): tCK = 4ns, CL=3, BL=4, tRCD = 3*tCK, tRC = 11*tCK, tRAS = 8*tCK
  Read: A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing
  50% of data changing at every burst

A=Activate, R=Read, W=Write, P=Precharge, N=NOP

### IDD7: Operating current: Four bank operation

1. Typical Case: VDD = 2.5V, T=25 °C for DDR266, 333; VDD = 2.6V , T=25 °C for DDR400, 500
2. Worst Case: VDD = 2.7V, T= 0 °C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns

- DDR266 (133Mhz, CL=2.5): tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK Read with autoprecharge
  Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
  50% of data changing at every burst
- DDR333(166Mhz, CL=2.5): tCK = 6ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
  Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
  50% of data changing at every burst
- DDR400(200Mhz, CL=3): tCK = 5ns, CL = 2, BL = 4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
  Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
  50% of data changing at every burst
- DDR500(250Mhz, CL=3): tCK = 4ns, CL = 2, BL = 4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
  Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
  50% of data changing at every burst

A=Activate, R=Read, W=Write, P=Precharge, N=NOP

## AC Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | VIH(AC) | VREF + 0.31 | | V | 1 |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals. | VIL(AC) | | VREF - 0.31 | V | 2 |
| Input Differential Voltage, CK and CK inputs | VID(AC) | 0.7 | VDDQ+0.6 | V | 3 |
| Input Crossing Point Voltage, CK and CK inputs | VIX(AC) | 0.5*VDDQ-0.2 | 0.5*VDDQ+0.2 | V | 4 |

**Note:**
1.Vih(max) = 4.2V. The overshoot voltage duration is ≤ 3ns at VDD.
2. Vil(min) = -1.5V. The undershoot voltage duration is ≤ 3ns at VSS.
3. VID is the magnitude of the difference between the input level on CK and the input on $\overline{\text{CK}}$.
4. The value of $V_{IX}$ is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

## *ELECTRICAL CHARACTERISTICS AND AC TIMING -Absolute Specifications*

( $V_{DDQ}$ = +2.5V ±0.2V, $V_{DD}$ = +2.5V ±0.2V )

| **AC CHARACTERISTICS** | | | **-6** | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | | **SYMBOL** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Access window of DQs from CK/$\overline{CK}$ | | $^tAC$ | -0.7 | 0.7 | ns | |
| CK high-level width | | $^tCH$ | 0.45 | 0.55 | $^tCK$ | 30 |
| CK low-level width | | $^tCL$ | 0.45 | 0.55 | $^tCK$ | 30 |
| Clock cycle time | CL = 3 | $^tCK$ (3) | 6 | 12 | ns | 52 |
| | CL = 2.5 | $^tCK$ (2.5) | 6 | 12 | ns | 52 |
| | CL = 2 | $^tCK$ (2) | 7.5 | 12 | ns | 52 |
| DQ and DM input hold time relative to DQS | | $^tDH$ | 0.45 | | ns | 26,31 |
| DQ and DM input setup time relative to DQS | | $^tDS$ | 0.45 | | ns | 26,31 |
| AUTO Precharge write recovery<br>+ precharge time | | $^tDAL$ | - | | $^tCK$ | 54 |
| DQ and DM input pulse width (for each input) | | $^tDIPW$ | 1.75 | | ns | 31 |
| Access window of DQS from CK/$\overline{CK}$ | | $^tDQSCK$ | -0.6 | 0.6 | ns | |
| DQS input high pulse width | | $^tDQSH$ | 0.35 | | $^tCK$ | |
| DQS input low pulse width | | $^tDQSL$ | 0.35 | | $^tCK$ | |
| DQS-DQ skew, DQS to last DQ valid,<br>per group, per access | | $^tDQSQ$ | | 0.40 | ns | 25,26 |
| Write command to first DQS latching transition | | $^tDQSS$ | 0.75 | 1.25 | $^tCK$ | |
| DQS falling edge to CK rising - setup time | | $^tDSS$ | 0.2 | | $^tCK$ | |
| DQS falling edge from CK rising - hold time | | $^tDSH$ | 0.2 | | $^tCK$ | |
| Half clock period | | $^tHP$ | $^tCH$,<br>$^tCL$ | | ns | 34 |
| Data-out high-impedance window from CK/$\overline{CK}$ | | $^tHZ$ | -0.7 | +0.7 | ns | 18 |
| Data-out low-impedance window from CK/$\overline{CK}$ | | $^tLZ$ | -0.7 | +0.7 | ns | 18 |

| AC CHARACTERISTICS | | -6 | | | |
|---|---|---|---|---|---|
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
| Address and control input hold time (fast slew rate) | $t_{IH_F}$ | 0.75 | | ns | 14 |
| Address and control input setup time (fast slew rate) | $t_{IS_F}$ | 0.75 | | ns | 14 |
| Address and control input hold time (slow slew rate) | $t_{IH_S}$ | 0.80 | | ns | 14 |
| Address and control input setup time (slow slew rate) | $t_{IS_S}$ | 0.80 | | ns | 14 |
| Control & Address input width (for each input) | $t_{IPW}$ | 2.2 | | ns | 53 |
| LOAD MODE REGISTER command cycle time | $t_{MRD}$ | 2 | | $t_{CK}$ | |
| DQ-DQS hold, DQS to first DQ to go non-valid, per access | $t_{QH}$ | $t_{HP}$ - $t_{QHS}$ | | ns | 25, 26 |
| Data hold skew factor | $t_{QHS}$ | | 0.55 | ns | |
| ACTIVE to PRECHARGE command | $t_{RAS}$ | 42 | 70,000 | ns | 35 |
| ACTIVE to READ with Auto precharge command | $t_{RAP}$ | 18 | | ns | 46 |
| ACTIVE to ACTIVE/AUTO REFRESH command period | $t_{RC}$ | 60 | | ns | |
| AUTO REFRESH command period | $t_{RFC}$ | 120 | | ns | 50 |
| ACTIVE to READ or WRITE delay | $t_{RCD}$ | 18 | | ns | |
| PRECHARGE command period | $t_{RP}$ | 18 | | ns | |
| DQS read preamble | $t_{RPRE}$ | 0.9 | 1.1 | $t_{CK}$ | 42 |
| DQS read postamble | $t_{RPST}$ | 0.4 | 0.6 | $t_{CK}$ | |
| ACTIVE bank a to ACTIVE bank b command | $t_{RRD}$ | 12 | | ns | |
| DQS write preamble | $t_{WPRE}$ | 0.25 | | $t_{CK}$ | |
| DQS write preamble setup time | $t_{WPRES}$ | 0 | | ns | 20, 21 |
| DQS write postamble | $t_{WPST}$ | 0.4 | 0.6 | $t_{CK}$ | 19 |
| Write recovery time | $t_{WR}$ | 15 | | ns | |
| Internal WRITE to READ command delay | $t_{WTR}$ | 1 | | $t_{CK}$ | |
| Data valid output window | na | $t_{QH}$ - $t_{DQSQ}$ | | ns | 25 |
| Average periodic refresh interval | $t_{REFI}$ | | 7.8 | us | |
| Terminating voltage delay to VDD | $t_{VTD}$ | 0 | | ns | |
| Exit SELF REFRESH to non-READ command | $t_{XSNR}$ | 75 | | ns | |
| Exit SELF REFRESH to READ command | $t_{XSRD}$ | 200 | | $t_{CK}$ | |

### SLEW RATE DERATING VALUES

( $V_{DDQ}$= +2.5V ±0.2V, $V_{DD}$ = +2.5V ±0.2V )

| | ADDRESS / COMMAND | | | |
|---|---|---|---|---|
| SLEW RATE | Δ $^t$IS | Δ $^t$IH | UNITS | NOTES |
| 0.500V / ns | 0 | 0 | ps | 14 |
| 0.400V / ns | +50 | +50 | ps | 14 |
| 0.300V / ns | +100 | +100 | ps | 14 |
| 0.200V / ns | +150 | +150 | ps | 14 |

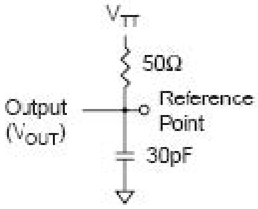
### SLEW RATE DERATING VALUES

( $V_{DDQ}$ = +2.5V ±0.2V, $V_{DD}$ = +2.5V ±0.2V )

| | Date, DQS, DM | | | |
|---|---|---|---|---|
| SLEW RATE | Δ $^t$DS | Δ $^t$DH | UNITS | NOTES |
| 0.500V / ns | 0 | 0 | ps | 31 |
| 0.400V / ns | +75 | +75 | ps | 31 |
| 0.300V / ns | +150 | +150 | ps | 31 |
| 0.200V / ns | +225 | +225 | ps | 31 |

**NOTES:**

1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load:



4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{REF}$ (or to the crossing point for CK/$\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. $V_{REF}$ is expected to equal $V_{DDQ}/2$ of the transmit-ting device and to track variations in the DC level of thesame. Peak-to-peak noise (non-common mode) on VREF may not exceed ±2 percent of the DC value. Thus, from $V_{DDQ}/2$, $V_{REF}$ is allowed ±25mV for DC error and an additional ±25mV for AC noise.

7. VTT is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors, is expected to be set equal to $V_{REF}$ and must track variations in the DC level of $V_{REF}$.

8. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

9. The value of VIX is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.

10. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at BL = 2 for -5, -6, and -75 with the outputs open.

11. Enables on-chip refresh and address counters.

12. IDD specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.

13. This parameter is sampled. $V_{DD}$ = +2.5V ±0.2V, $V_{DDQ}$ = +2.5V ±0.2V, $V_{REF} = V_{SS}$, f = 100 MHz, T A = 25°C, VOUT(DC) = $V_{DDQ}/2$, VOUT (peak to peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.

14. Command/Address input slew rate = 0.5V/ns. For -5, -6, and -75 with slew rates 1V/ns and faster, $^{t}$IS and $^{t}$IH are reduced to 900ps. If the slew rate is less than 0.5V/ns, timing must be derated: $^{t}$IS and $^{t}$IH has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. If the slew rate exceeds 4.5V/ns, functionality is uncertain.

15. The CK/$\overline{CK}$ input reference level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK/$\overline{CK}$ is $V_{REF}$.

16. Inputs are not recognized as valid until $V_{REF}$ stabilizes. Exception: during the period before $V_{REF}$ stabilizes, CKE •0.3 x V is recognized as LOW.

17. The output timing reference level, as measured at the timing reference point indicated in Note 3, is $V_{TT}$.

18. $^{t}$HZ and $^{t}$LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).

19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.

21. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}$DQSS.

22. MIN ($^{t}$RC or $^{t}$RFC) for IDD measurements is the smallest multiple of $^{t}$CK that meets the minimum absolute value for the respective parameter. $^{t}$RAS (MAX) for IDD measurements is the largest multiple of $^{t}$CK that meets the maximum absolute value for $^{t}$RAS.

23. The refresh period 64ms. This equates to an average refresh rate of 7.8μs.

24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

25. The valid data window is derived by achieving other specifications - $^{t}$HP ($^{t}$CK/2), $^{t}$DQSQ, and $^{t}$QH ($^{t}$QH = $^{t}$HP - $^{t}$QHS). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.

26. Referenced to each output group: x4 = DQS with DQ0-DQ3; x8 = DQS with DQ0-DQ7; x16 = LDQS with DQ0-DQ7; and UDQS with DQ8-DQ15.

27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period ($^t$RFC [MIN]) else CKE is LOW (i.e., during standby).

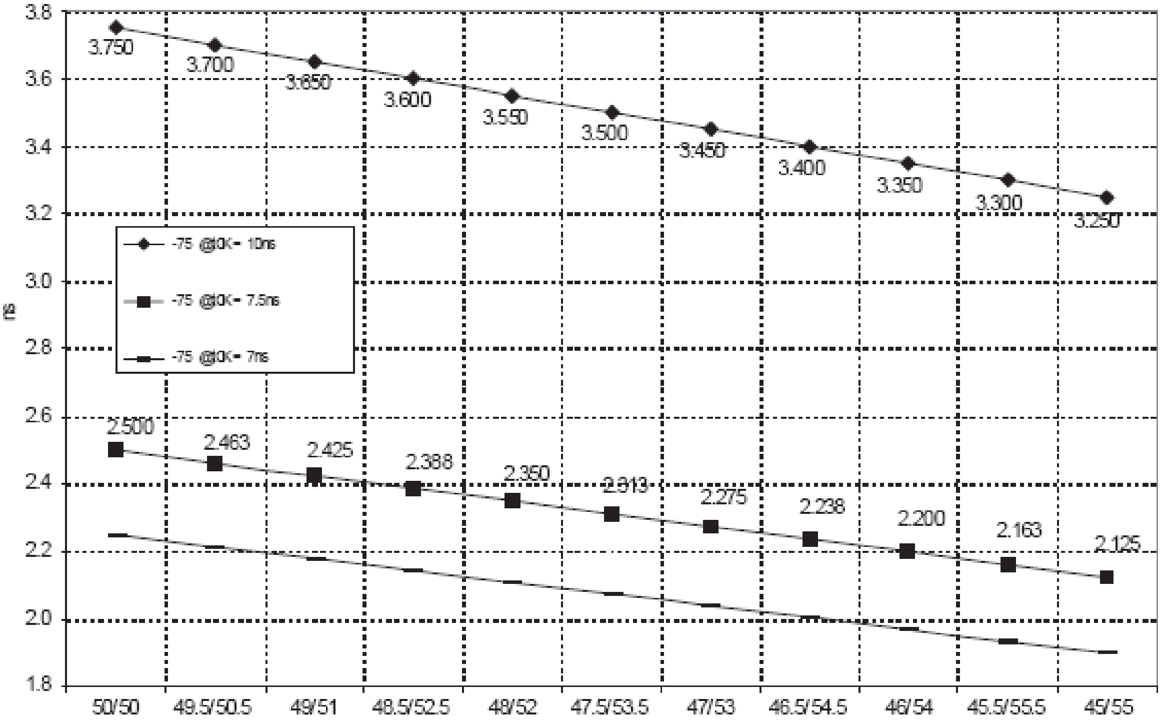
28. To maintain a valid level, the transitioning edge of the input must:
    a) Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
    b) Reach at least the target AC level.
    c) After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).

29. The Input capacitance per pin group will not differ by more than this maximum amount for any given device..

30. CK and $\overline{CK}$ input slew rate must be •1V/ns.

31. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to $^t$DS and $^t$DH for each 100mv/ns reduction in slew rate. If slew rate exceeds 4V/ns, functionality is uncertain.

32. VDD must not vary more than 4% if CKE is not active while any bank is active.



33. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.

34. $^t$HP min is the lesser of $^t$CL minimum and $^t$CH minimum actually applied to the device CK and CK/ inputs, collectively during bank active.

35. READs and WRITEs with auto precharge are not allowed to be issued until $^t$RAS(MIN) can be satisfied prior to the internal precharge command being issued.

36. Applies to x16 only. First DQS (LDQS or UDQS) to transition to last DQ ($DQ_0$-$DQ_{15}$) to transition valid. Initial JEDEC specifications suggested this to be same as $^t$DQSQ.

37. Normal Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure A.

    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but no guaranteed, to lie within the inner bounding lines of the V-I curve of Figure A.

c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure B.

d)The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure B.

e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 Volt, and at the same voltage and temperature.

f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0 Volt.

38. Reduced Output Drive Curves:
    a) The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure C.

    b) The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure C.

    c) The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure D.

    d)The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure D.

    e) The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between .71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0 V, and at the same voltage.

    f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0 V.

39. The voltage levels used are derived from the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.

40. VIH overshoot: VIH(MAX) = $V_{DDQ}$+1.5V for a pulse width •3ns and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL(MIN) = -1.5V for a pulse width •3ns and the pulse width can not be greater than 1/3 of the cycle rate.

41. $V_{DD}$ and $V_{DDQ}$ must track each other.

42. Note 42 is not used.

43. Note 43 is not used.

44. During initialization, $V_{DDQ}$, $V_{TT}$, and $V_{REF}$ must be equal to or less than $V_{DD}$ + 0.3V. Alternatively, $V_{TT}$ may be 1.35V maximum during power up, even if $V_{DD}$ /$V_{DDQ}$ are 0 volts, provided a minimum of 42 ohms of series resistance is used between the $V_{TT}$ supply and the input pin.

45. Note 45 is not used.

46. $^{t}$RAP •t RCD.

47. Note 47 is not used.

48. Random addressing changing 50% of data changing at every transfer.

49. Random addressing changing 100% of data changing at every transfer.

50. CKE must be active (high) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until $t_{REF}$ later.

51. IDD2N specifies the DQ, DQS, and DM to be driven to a valid high or low logic level. IDD2Q is similar to IDD2F except IDD2Q specifies the address and control inputs to remain stable. Although IDD2F, IDD2N, and IDD2Q are similar, IDD2F is "worst case."

52. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles.

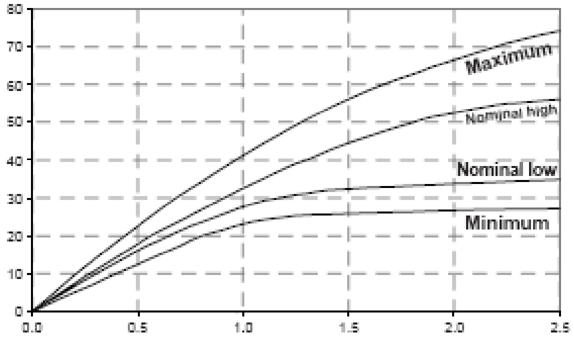
53. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

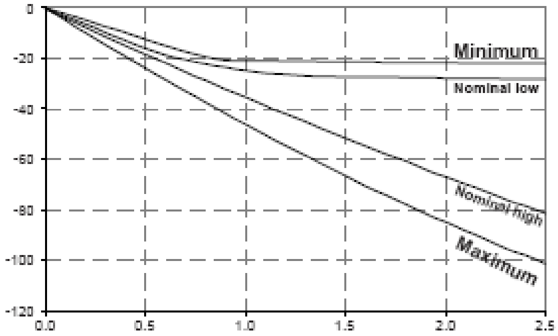
54. ${}^{t}$DAL =(${}^{t}$WR/ ${}^{t}$CK) + (${}^{t}$RP/ ${}^{t}$CK)

For each of the terms above, if not already an integer, round to the next highest integer.

For example: For DDR266B at CL=2.5 and ${}^{t}$CK=7.5ns

${}^{t}$DAL=((15ns /7.5ns) + (20ns/ 7.5ns)) clocks=((2)+(3)) clocks=5 clocks

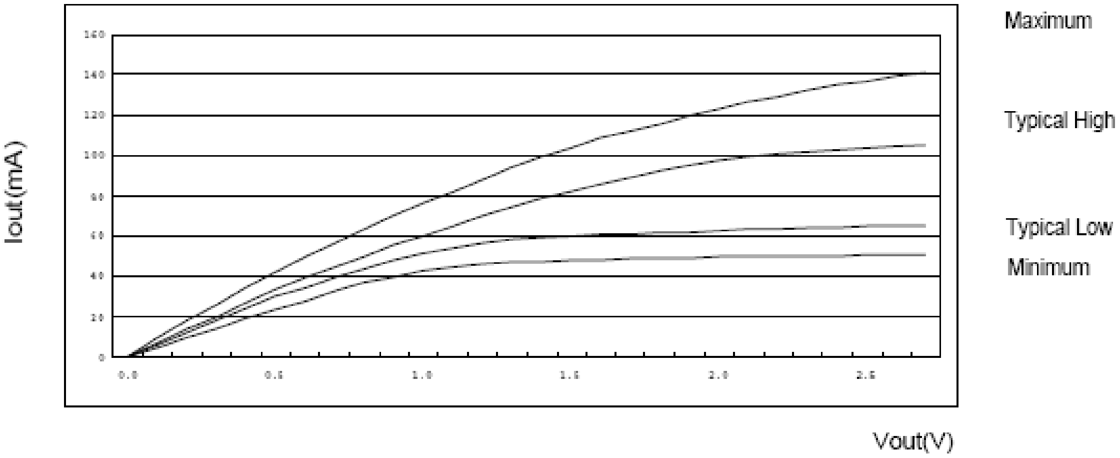




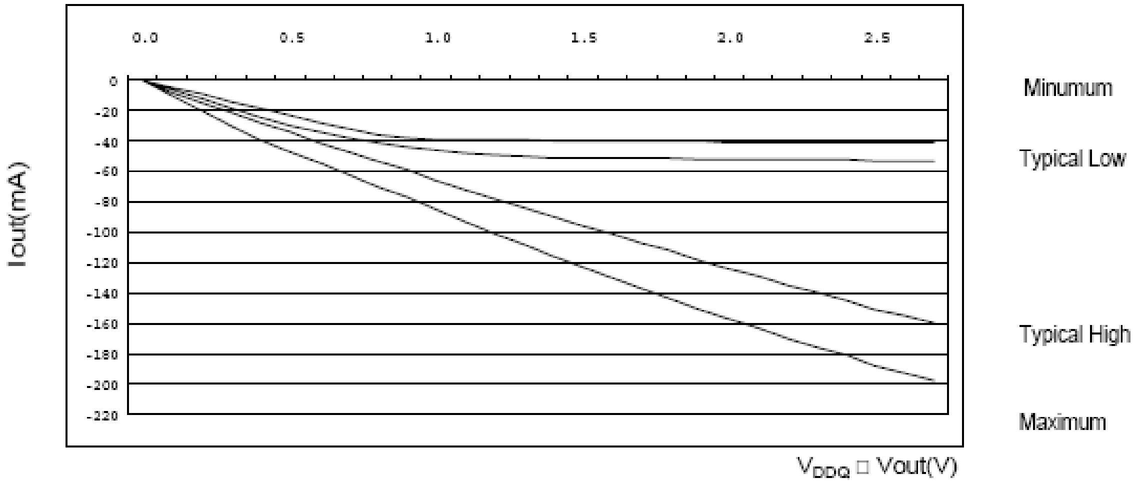
## *IBIS: I/V Characteristics for Input and Output Buffers*

### Normal strength driver

1. The nominal pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.
2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.



3. The nominal pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.
4. The Full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure b.



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2
6. The Full variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

Figure 25. I/V characteristics for input/output buffers:Pull up(above) and pull down(below)

| | Pulldown Current (mA) | | | | Pullup Current (mA) | | | |
|---|---|---|---|---|---|---|---|---|
| Voltage (V) | Typical Low | Typical High | Minimum | Maximum | Typical Low | Typical High | Minimum | Maximum |
| 0.1 | 6.0 | 6.8 | 4.6 | 9.6 | -6.1 | -7.6 | -4.6 | -10.0 |
| 0.2 | 12.2 | 13.5 | 9.2 | 18.2 | -12.2 | -14.5 | -9.2 | -20.0 |
| 0.3 | 18.1 | 20.1 | 13.8 | 26.0 | -18.1 | -21.2 | -13.8 | -29.8 |
| 0.4 | 24.1 | 26.6 | 18.4 | 33.9 | -24.0 | -27.7 | -18.4 | -38.8 |
| 0.5 | 29.8 | 33.0 | 23.0 | 41.8 | -29.8 | -34.1 | -23.0 | -46.8 |
| 0.6 | 34.6 | 39.1 | 27.7 | 49.4 | -34.3 | -40.5 | -27.7 | -54.4 |
| 0.7 | 39.4 | 44.2 | 32.2 | 56.8 | -38.1 | -46.9 | -32.2 | -61.8 |
| 0.8 | 43.7 | 49.8 | 36.8 | 63.2 | -41.1 | -53.1 | -36.0 | -69.5 |
| 0.9 | 47.5 | 55.2 | 39.6 | 69.9 | -41.8 | -59.4 | -38.2 | -77.3 |
| 1.0 | 51.3 | 60.3 | 42.6 | 76.3 | -46.0 | -65.5 | -38.7 | -85.2 |
| 1.1 | 54.1 | 65.2 | 44.8 | 82.5 | -47.8 | -71.6 | -39.0 | -93.0 |
| 1.2 | 56.2 | 69.9 | 46.2 | 88.3 | -49.2 | -77.6 | -39.2 | -100.6 |
| 1.3 | 57.9 | 74.2 | 47.1 | 93.8 | -50.0 | -83.6 | -39.4 | -108.1 |
| 1.4 | 59.3 | 78.4 | 47.4 | 99.1 | -50.5 | -89.7 | -39.6 | -115.5 |
| 1.5 | 60.1 | 82.3 | 47.7 | 103.8 | -50.7 | -95.5 | -39.9 | -123.0 |
| 1.6 | 60.5 | 85.9 | 48.0 | 108.4 | -51.0 | -101.3 | -40.1 | -130.4 |
| 1.7 | 61.0 | 89.1 | 48.4 | 112.1 | -51.1 | -107.1 | -40.2 | -136.7 |
| 1.8 | 61.5 | 92.2 | 48.9 | 115.9 | -51.3 | -112.4 | -40.3 | -144.2 |
| 1.9 | 62.0 | 95.3 | 49.1 | 119.6 | -51.5 | -118.7 | -40.4 | -150.5 |
| 2.0 | 62.5 | 97.2 | 49.4 | 123.3 | -51.6 | -124.0 | -40.5 | -156.9 |
| 2.1 | 62.9 | 99.1 | 49.6 | 126.5 | -51.8 | -129.3 | -40.6 | -163.2 |
| 2.2 | 63.3 | 100.9 | 49.8 | 129.5 | -52.0 | -134.6 | -40.7 | -169.6 |
| 2.3 | 63.8 | 101.9 | 49.9 | 132.4 | -52.2 | -139.9 | -40.8 | -176.0 |
| 2.4 | 64.1 | 102.8 | 50.0 | 135.0 | -52.3 | -145.2 | -40.9 | -181.3 |
| 2.5 | 64.6 | 103.8 | 50.2 | 137.3 | -52.5 | -150.5 | -41.0 | -187.6 |
| 2.6 | 64.8 | 104.6 | 50.4 | 139.2 | -52.7 | -155.3 | -41.1 | -192.9 |
| 2.7 | 65.0 | 105.4 | 50.5 | 140.8 | -52.8 | -160.1 | -41.2 | -198.2 |

Table 17. Pull down and pull up current values

Temperature (Tambient)

| | |
|---|---|
| Typical | 25°C |
| Minimum | 0°C for normal, -40°C for Industrial |
| Maximum | 70°C for normal, 85°C for Industrial |

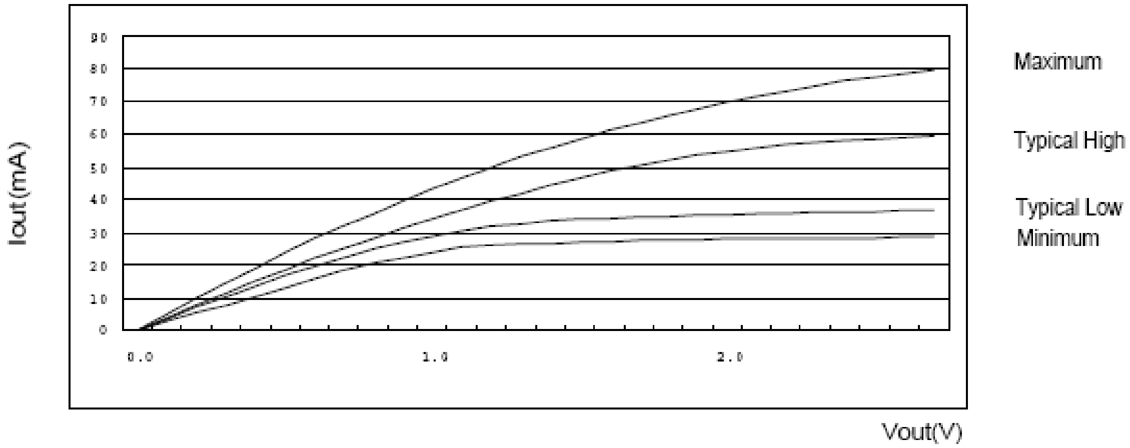
| | |
|---|---|
| Vdd/Vddq | DDR333/DDR266 |
| Typical | 2.5V |
| Minimum | 2.3V |
| Maximum | 2.7V |

The above characteristics are specified under best, worst and normal process variation/conditions

### *Half strength driver*

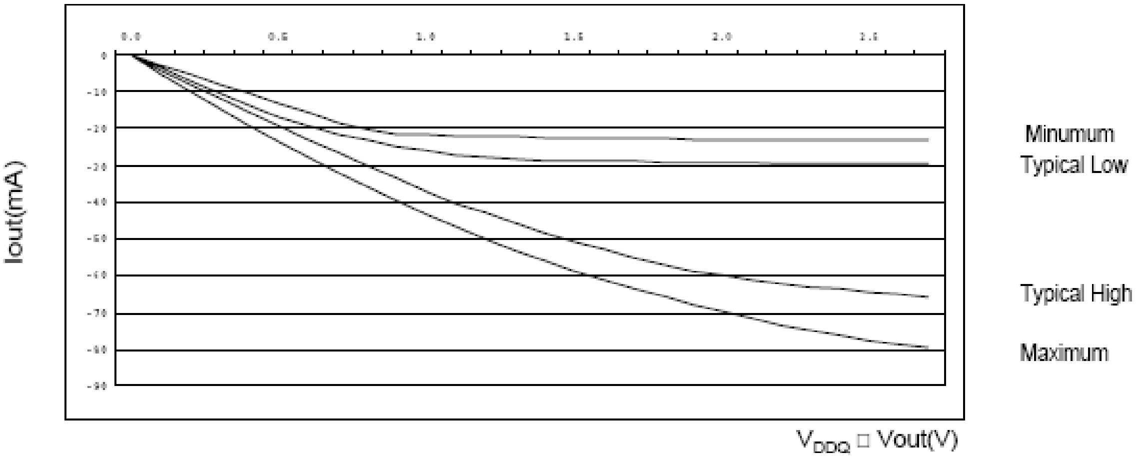
1. The nominal pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of Figure a.

2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines the of the V-I curve of Figure a.



3. The nominal pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below Figure b.

4. The Full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure b.



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2

6. The Full variation in the ratio of the nominal pullup to pulldown current should be unity ±10%, for device drain to source voltages from 0 to VDDQ/2

**Figure 26. I/V characteristics for input/output buffers:Pull up(above) and pull down(below)**

| | Pulldown Current (mA) | | | | Pullup Current (mA) | | | |
|---|---|---|---|---|---|---|---|---|
| Voltage (V) | Typical Low | Typical High | Minimum | Maximum | Typical Low | Typical High | Minimum | Maximum |
| 0.1 | 3.4 | 3.8 | 2.6 | 5.0 | -3.5 | -4.3 | -2.6 | -5.0 |
| 0.2 | 6.9 | 7.6 | 5.2 | 9.9 | -6.9 | -8.2 | -5.2 | -9.9 |
| 0.3 | 10.3 | 11.4 | 7.8 | 14.6 | -10.3 | -12.0 | -7.8 | -14.6 |
| 0.4 | 13.6 | 15.1 | 10.4 | 19.2 | -13.6 | -15.7 | -10.4 | -19.2 |
| 0.5 | 16.9 | 18.7 | 13.0 | 23.6 | -16.9 | -19.3 | -13.0 | -23.6 |
| 0.6 | 19.6 | 22.1 | 15.7 | 28.0 | -19.4 | -22.9 | -15.7 | -28.0 |
| 0.7 | 22.3 | 25.0 | 18.2 | 32.2 | -21.5 | -26.5 | -18.2 | -32.2 |
| 0.8 | 24.7 | 28.2 | 20.8 | 35.8 | -23.3 | -30.1 | -20.4 | -35.8 |
| 0.9 | 26.9 | 31.3 | 22.4 | 39.5 | -24.8 | -33.6 | -21.6 | -39.5 |
| 1.0 | 29.0 | 34.1 | 24.1 | 43.2 | -26.0 | -37.1 | -21.9 | -43.2 |
| 1.1 | 30.6 | 36.9 | 25.4 | 46.7 | -27.1 | -40.3 | -22.1 | -46.7 |
| 1.2 | 31.8 | 39.5 | 26.2 | 50.0 | -27.8 | -43.1 | -22.2 | -50.0 |
| 1.3 | 32.8 | 42.0 | 26.6 | 53.1 | -28.3 | -45.8 | -22.3 | -53.1 |
| 1.4 | 33.5 | 44.4 | 26.8 | 56.1 | -28.6 | -48.4 | -22.4 | -56.1 |
| 1.5 | 34.0 | 46.6 | 27.0 | 58.7 | -28.7 | -50.7 | -22.6 | -58.7 |
| 1.6 | 34.3 | 48.6 | 27.2 | 61.4 | -28.9 | -52.9 | -22.7 | -61.4 |
| 1.7 | 34.5 | 50.5 | 27.4 | 63.5 | -28.9 | -55.0 | -22.7 | -63.5 |
| 1.8 | 34.8 | 52.2 | 27.7 | 65.6 | -29.0 | -56.8 | -22.8 | -65.6 |
| 1.9 | 35.1 | 53.9 | 27.8 | 67.7 | -29.2 | -58.7 | -22.9 | -67.7 |
| 2.0 | 35.4 | 55.0 | 28.0 | 69.8 | -29.2 | -60.0 | -22.9 | -69.8 |
| 2.1 | 35.6 | 56.1 | 28.1 | 71.6 | -29.3 | -61.2 | -23.0 | -71.6 |
| 2.2 | 35.8 | 57.1 | 28.2 | 73.3 | -29.5 | -62.4 | -23.0 | -73.3 |
| 2.3 | 36.1 | 57.7 | 28.3 | 74.9 | -29.5 | -63.1 | -23.1 | -74.9 |
| 2.4 | 36.3 | 58.2 | 28.3 | 76.4 | -29.6 | -63.8 | -23.2 | -76.4 |
| 2.5 | 36.5 | 58.7 | 28.4 | 77.7 | -29.7 | -64.4 | -23.2 | -77.7 |
| 2.6 | 36.7 | 59.2 | 28.5 | 78.8 | -29.8 | -65.1 | -23.3 | -78.8 |
| 2.7 | 36.8 | 59.6 | 28.6 | 79.7 | -29.9 | -65.8 | -23.3 | -79.7 |

**Table 18. Pull down and pull up current values**

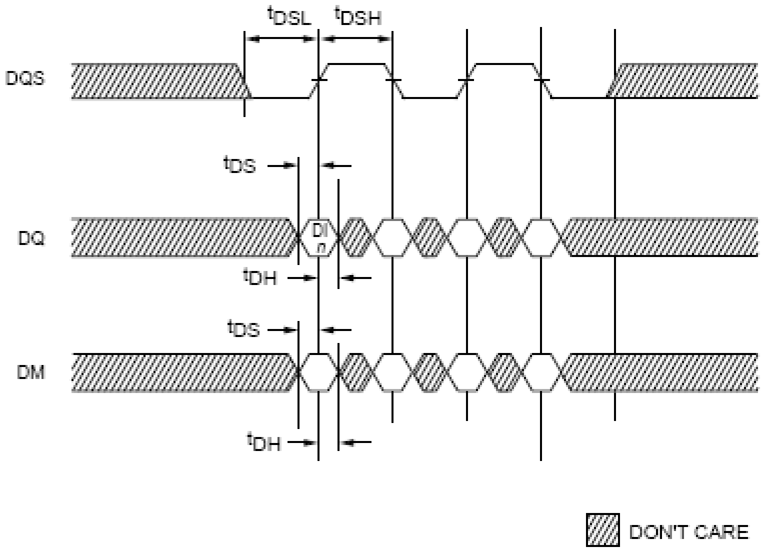
Temperature (Tambient)

| | |
|---|---|
| Typical | 25°C |
| Minimum | 0°C for normal, -40°C for Industrial |
| Maximum | 70°C for normal, 85°C for Industrial |

| Vdd/Vddq | DDR333/DDR266 |
|---|---|
| Typical | 2.5V |
| Minimum | 2.3V |
| Maximum | 2.7V |

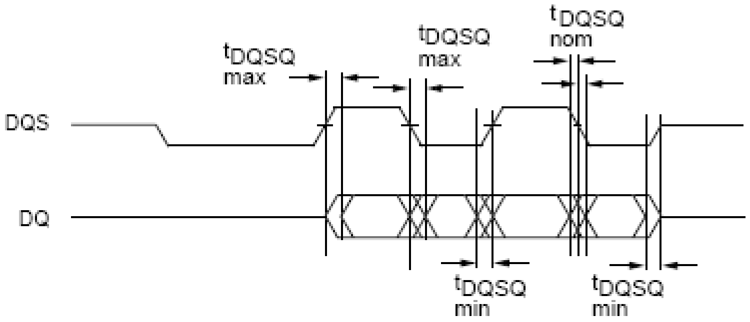
The above characteristics are specified under best, worst and normal process variation/conditions

## Figure 36 - DATA INPUT (WRITE) TIMING

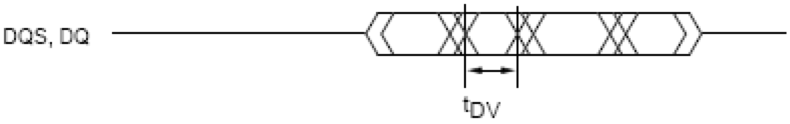


DI *n* = Data In for column *n*
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI *n*

## Figure 37 - DATA OUTPUT (READ) TIMING

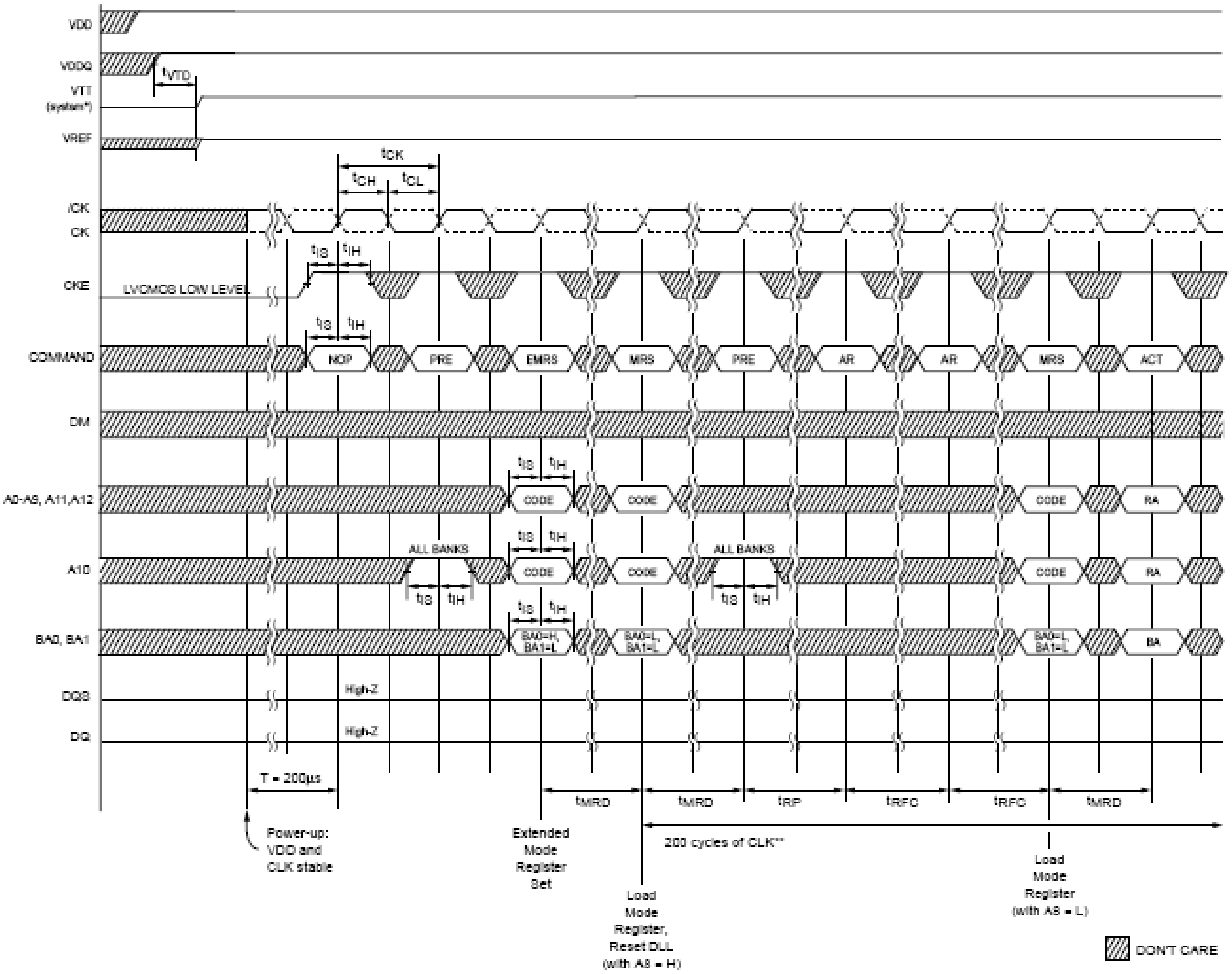


tDQSQ max occurs when DQS is the earliest among DQS and DQ signals to transition.
tDQSQ min occurs when DQS is the latest among DQS and DQ signals to transition.
tDQSQ nom, shown for reference, occurs when DQS transitions in the center among DQ signal transitions.



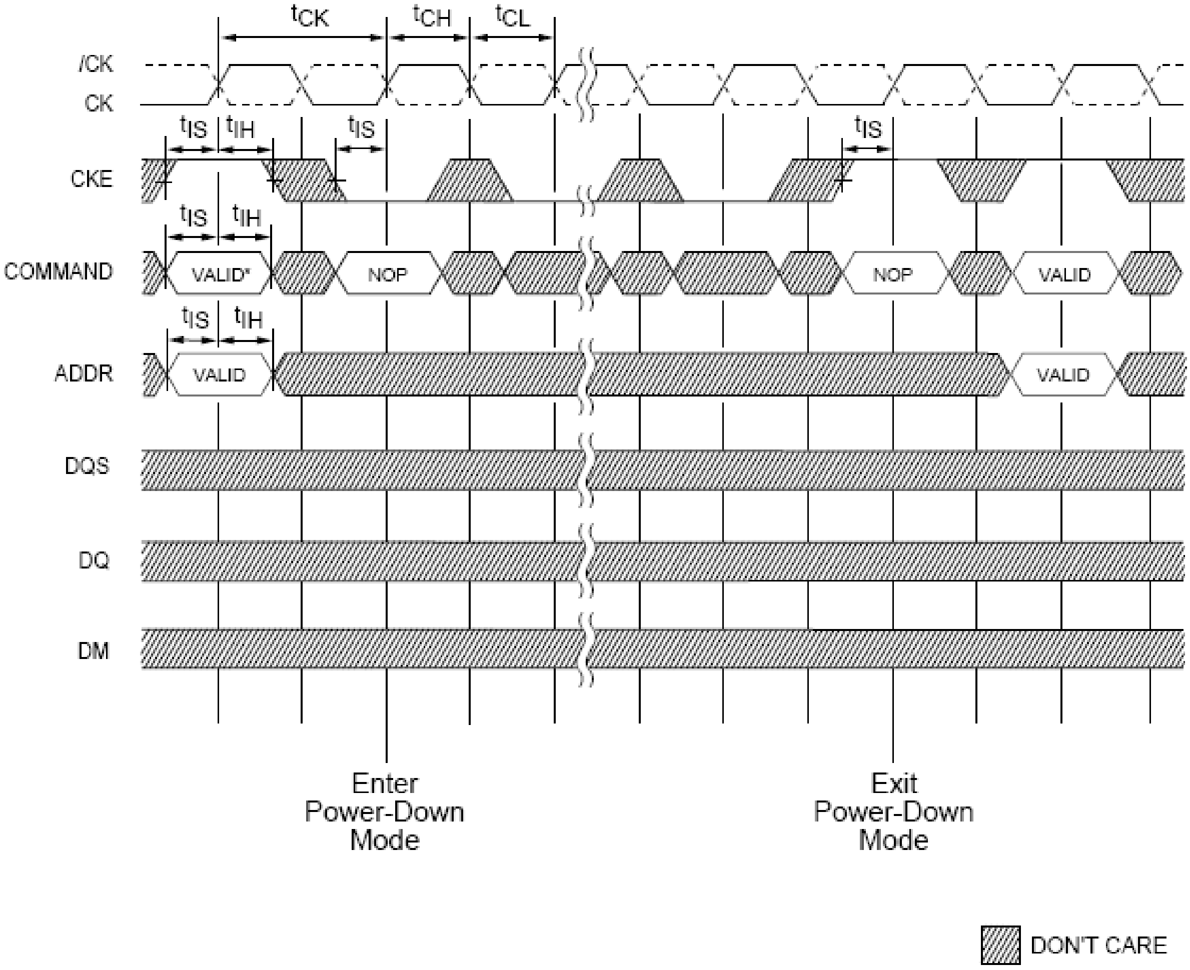
Burst Length = 4 in the case shown

Figure 38 - INITIALIZE AND MODE REGISTER SETS



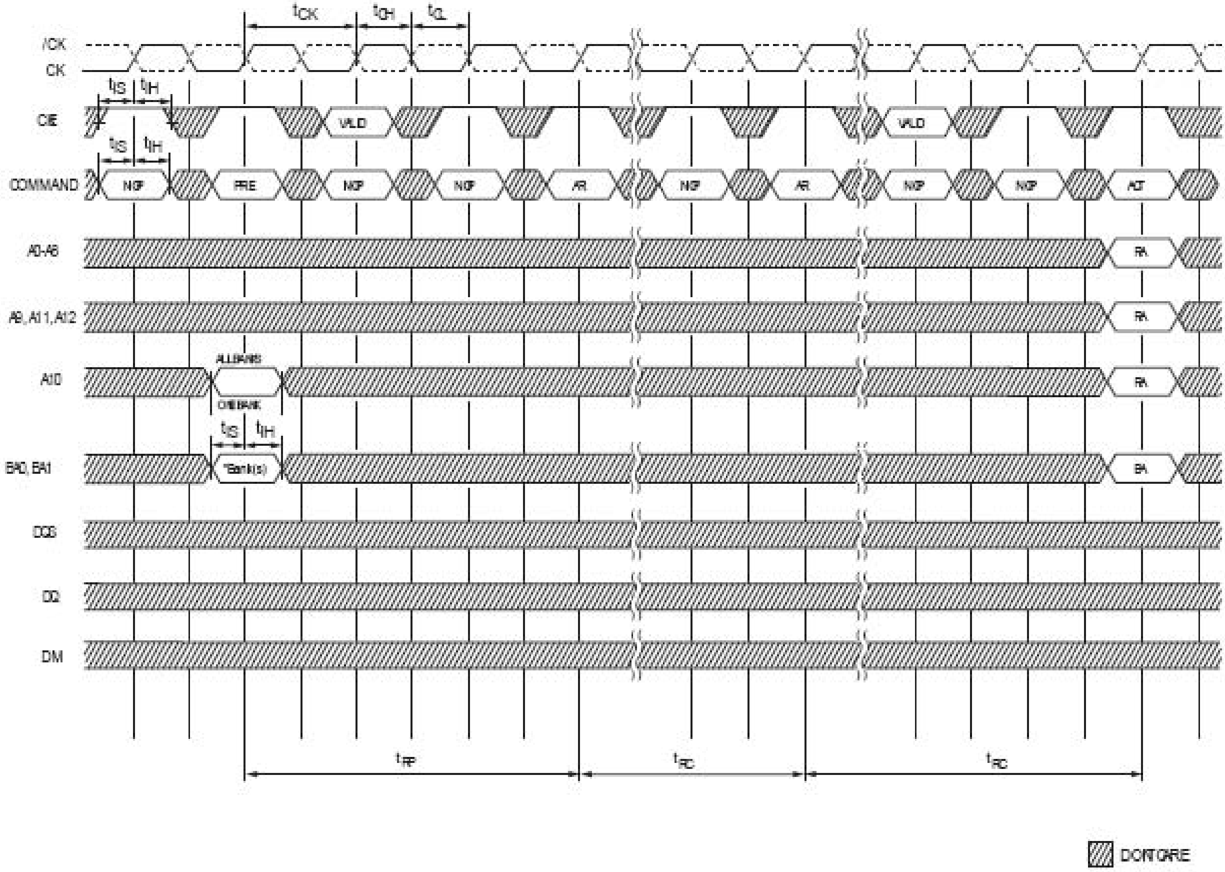
* = VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up.
** = tMRD is required before any command can be applied, and 200 cycles of CK are required before a READ command can be applied.
The two Auto Refresh commands may be moved to follow the first MRS, but precede the second PRECHARGE ALL command.

Figure 39 - POWER-DOWN MODE



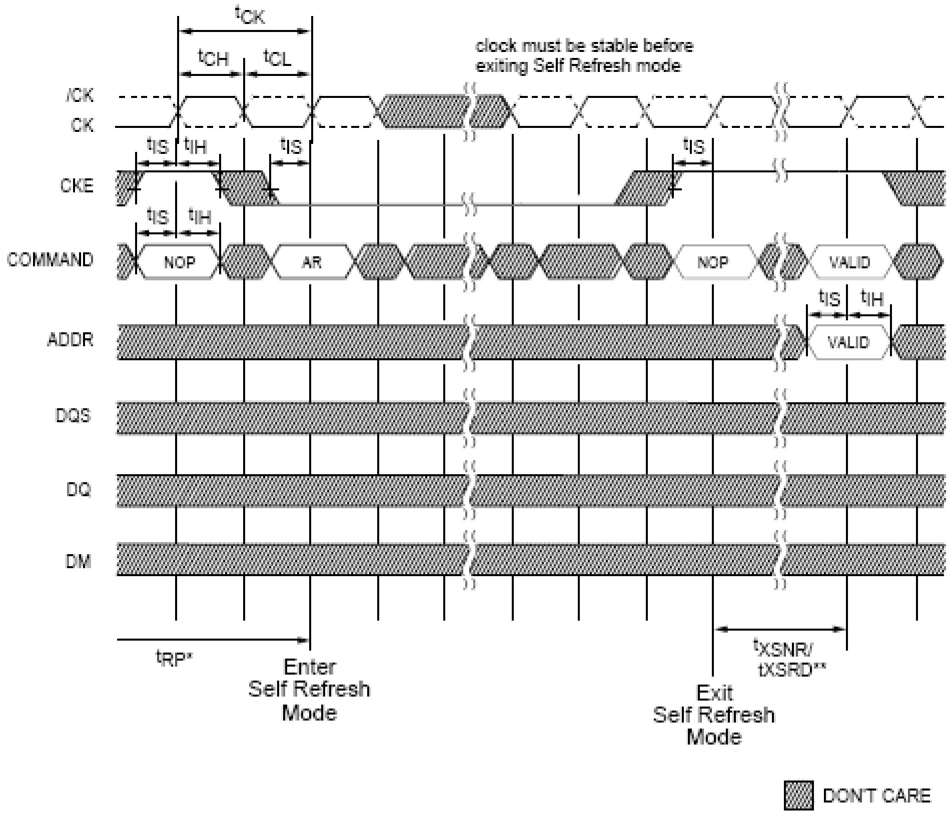
No column accesses are allowed to be in progress at the time Power-Down is entered
* = If this command is a PRECHARGE (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is Active Power Down.

## Figure 40 - AUTO REFRESH MODE



* = "Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e. must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible at these times
DM, DQ and DQS signals are all "Don't Care"/High-Z for operations shown

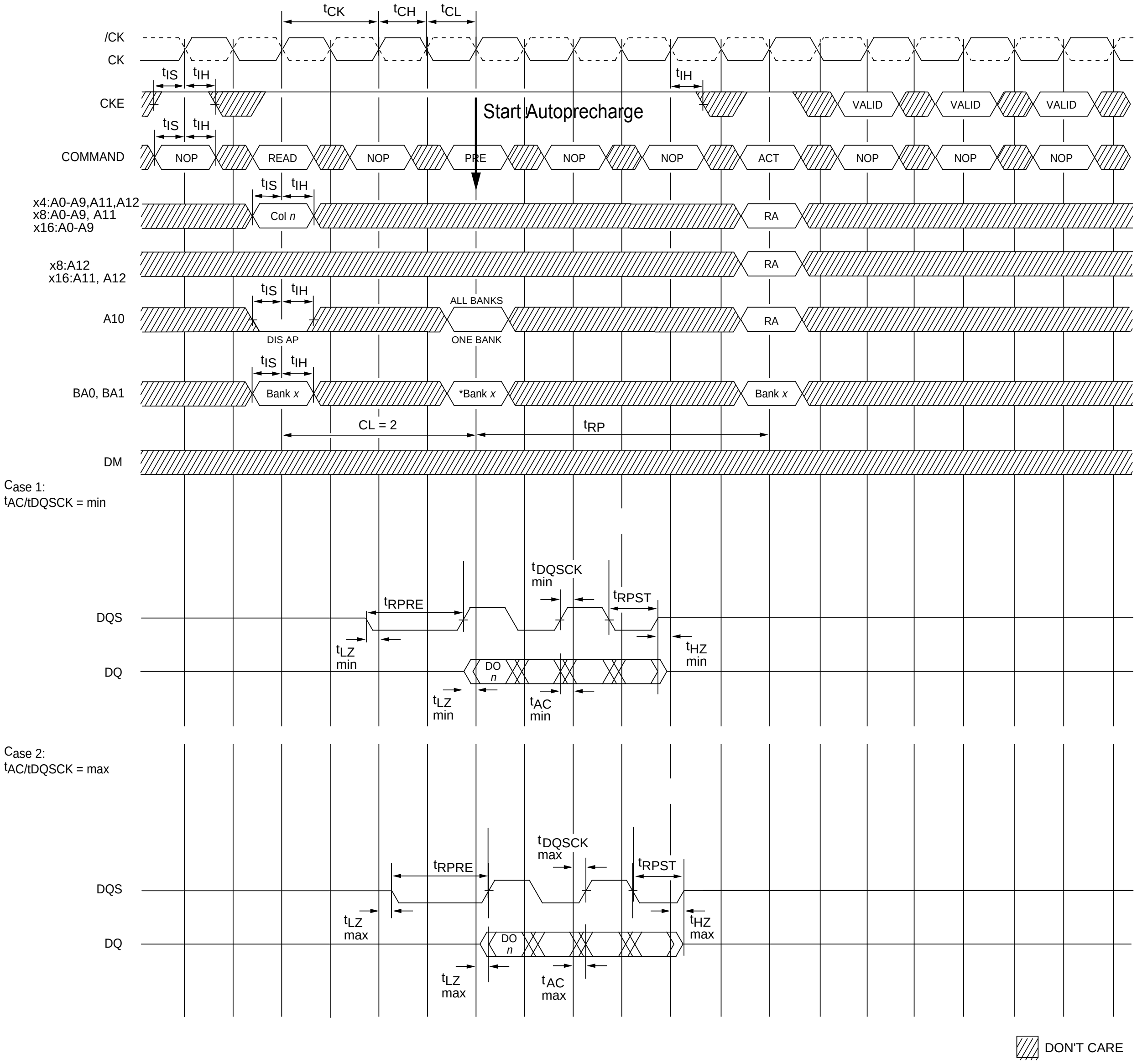
Figure 41 - SELF REFRESH MODE



* = Device must be in the "All banks idle" state prior to entering Self Refresh mode

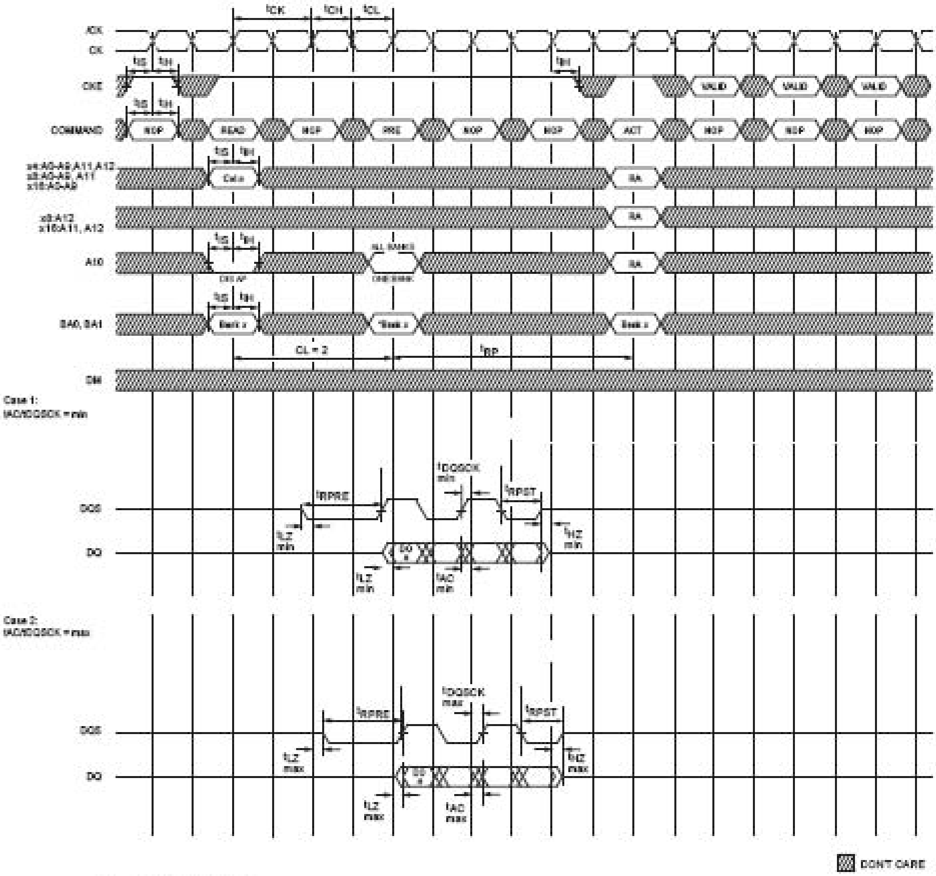
** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CLK) are required before a READ command can be applied.

**Figure 42 - READ - WITHOUT AUTO PRECHARGE**



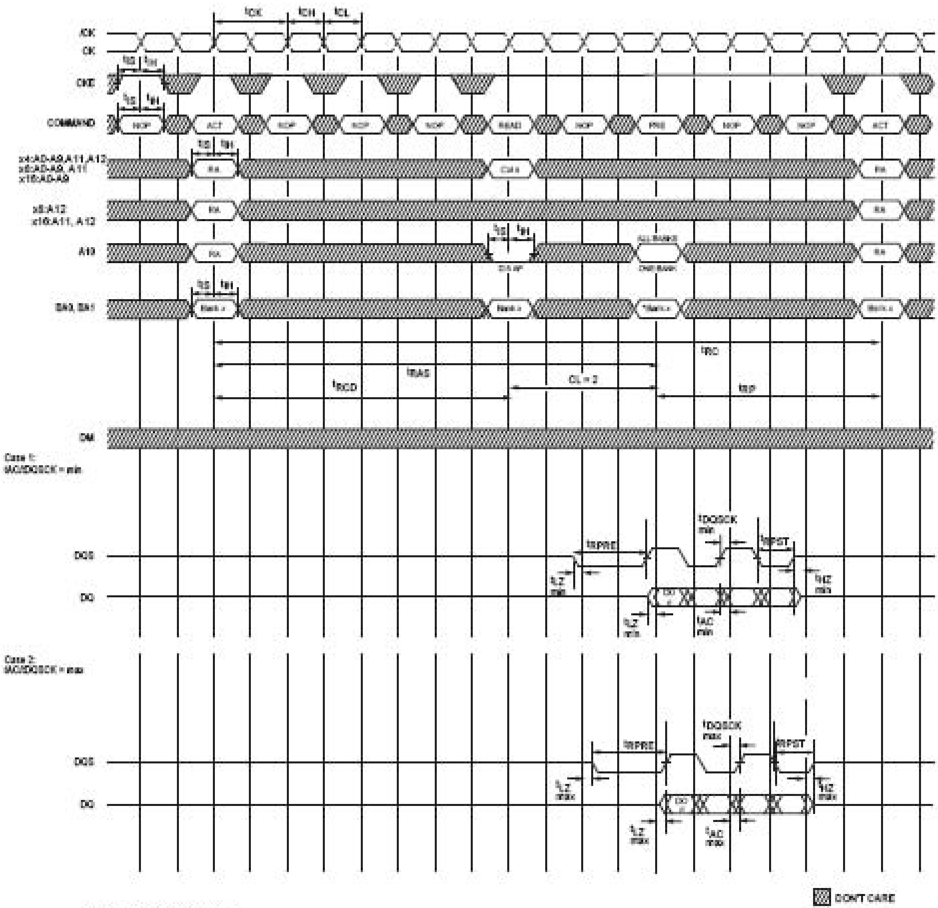
DO *n* = Data Out from column *n*
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO *n*
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 43 - READ - WITH AUTO PRECHARGE



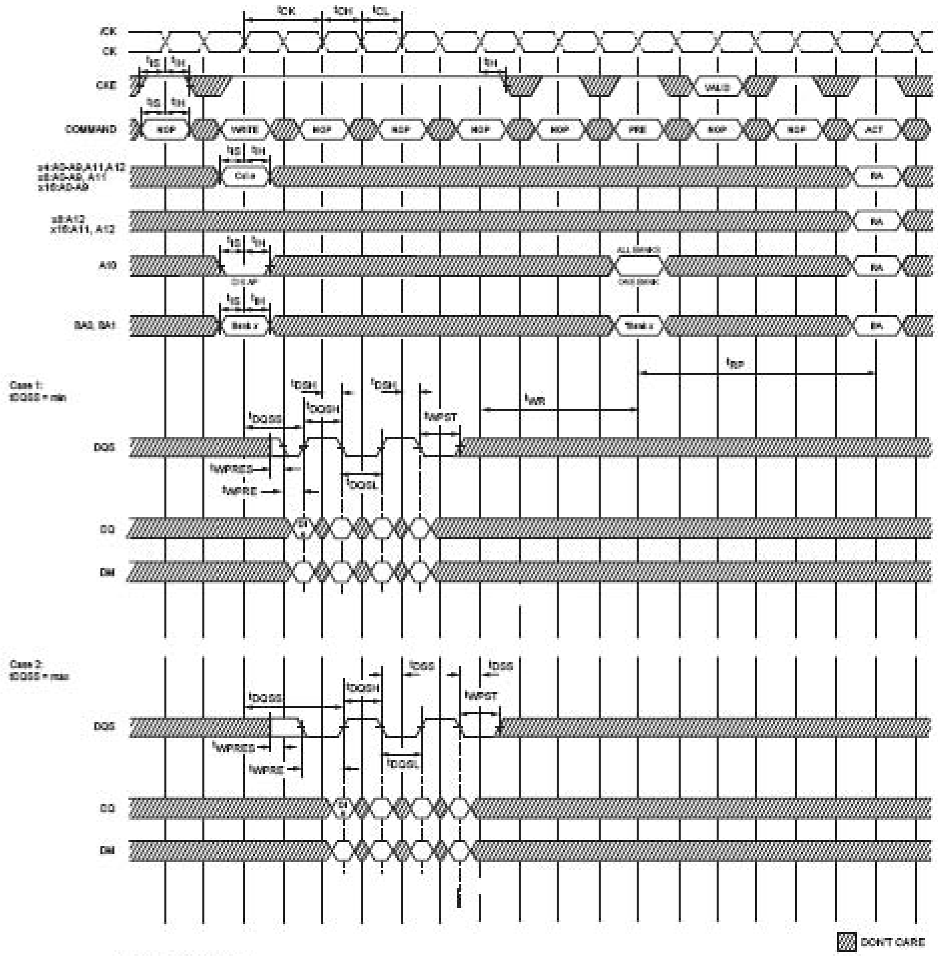
DO *n* = Data Out from column *n*
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO *n*
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times

Figure 44 - BANK READ ACCESS



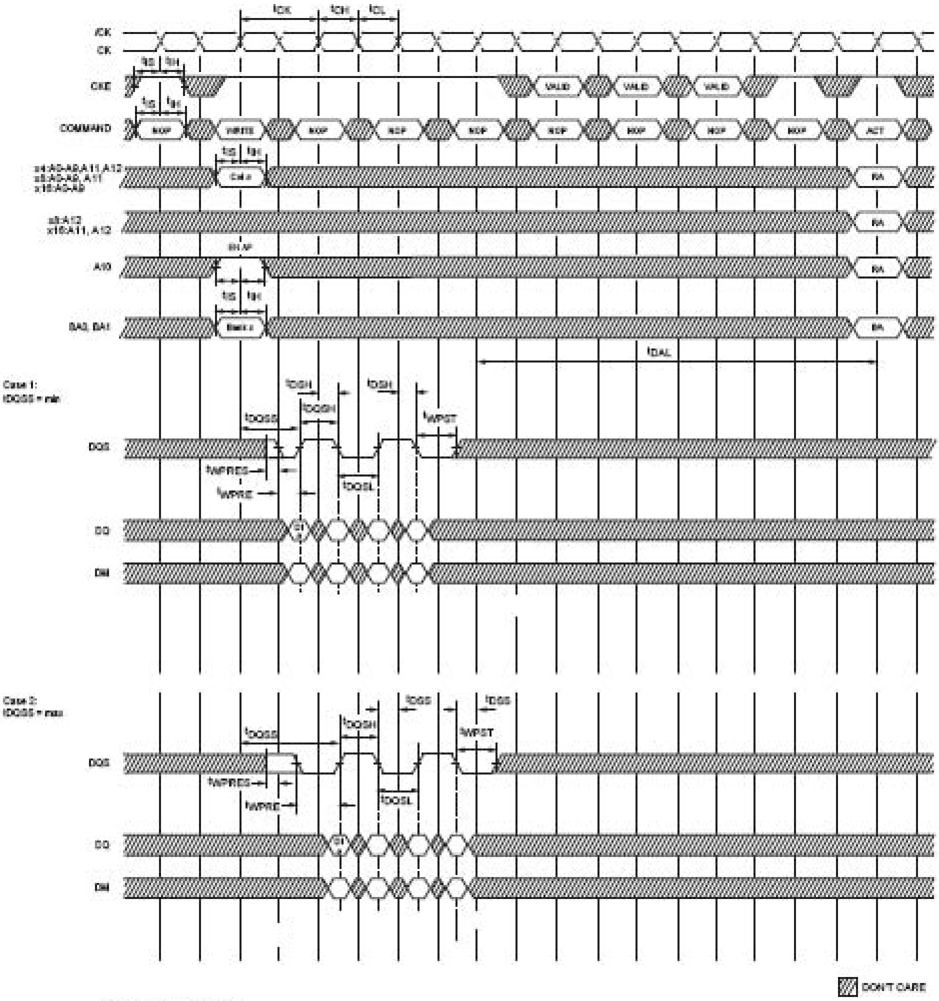
DO n = Data Out from column n
Burst Length = 4 in the case shown
3 subsequent elements of Data Out are provided in the programmed order following DO n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other commands may be valid at these times
Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Figure 45 - WRITE - WITHOUT AUTO PRECHARGE



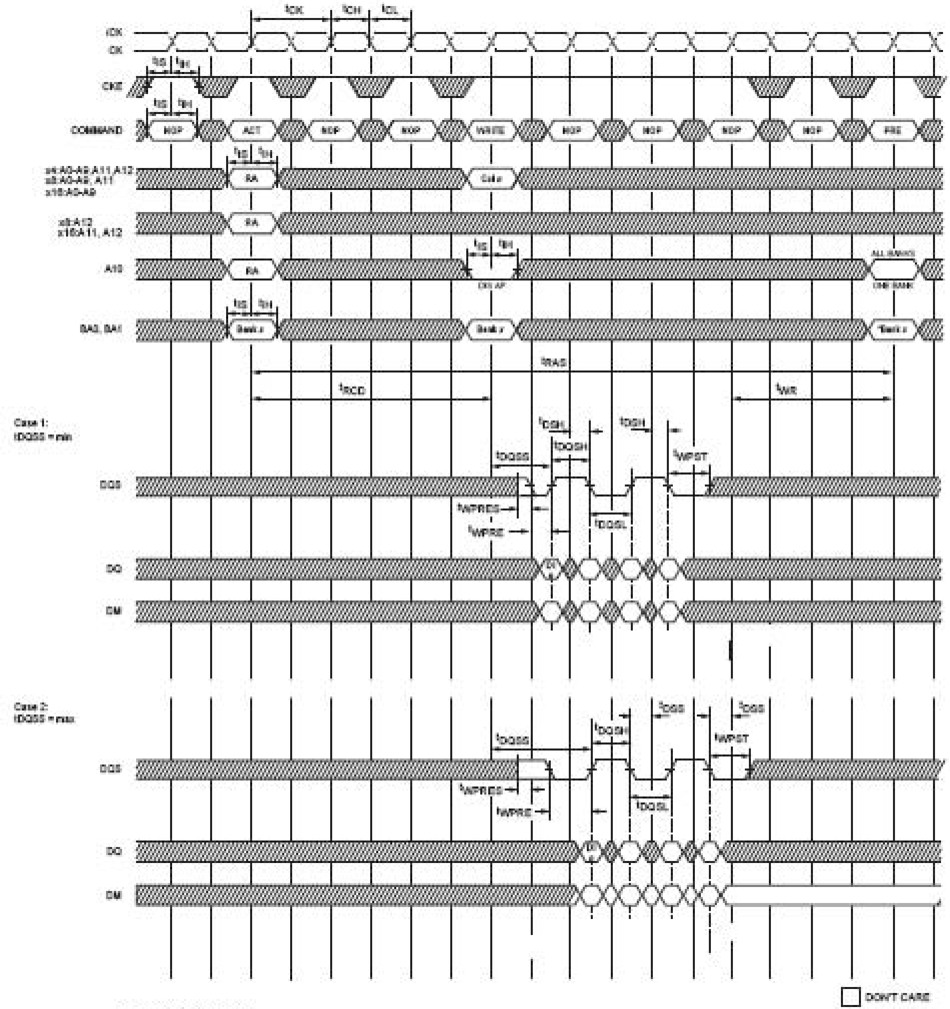
DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

Figure 46 - WRITE - WITH AUTO PRECHARGE



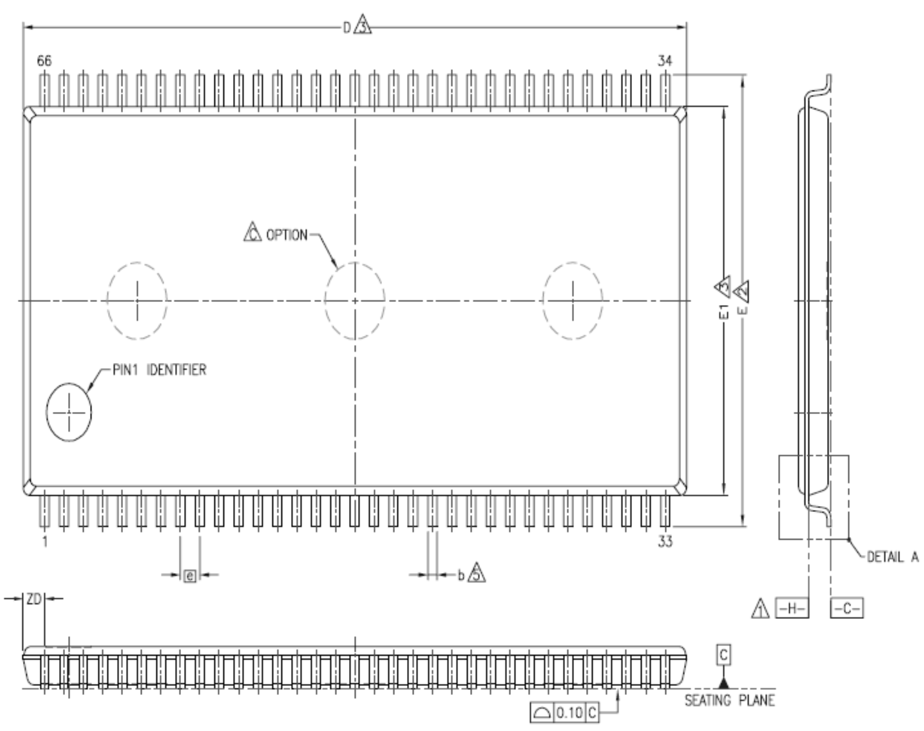
DI n = Data in for column n  
Burst Length = 4 in the case shown  
3 subsequent elements of Data In are applied in the programmed order following DI n  
EN AP = Enable Autoprecharge  
ACT = ACTIVE, RA = Row Address, BA = Bank Address  
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

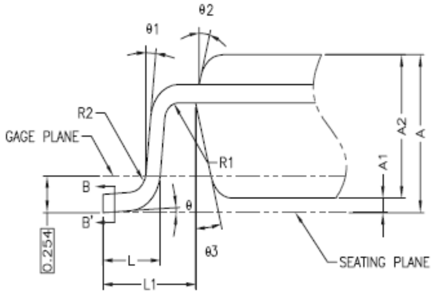
Figure 47 - BANK WRITE ACCESS



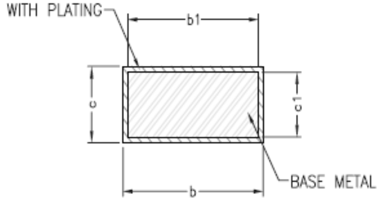
DI n = Data In for column n
Burst Length = 4 in the case shown
3 subsequent elements of Data In are applied in the programmed order following DI n
DIS AP = Disable Autoprecharge
* = "Don't Care", if A10 is HIGH at this point
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address
NOP commands are shown for ease of illustration; other valid commands may be possible at these times

## *Package Diagram*
## 66-Pin TSOP-II (400 mil)





DETAIL A



SECTION B–B' △4

| SYM. | DIMENSION (MM) | | | DIMENSION (INCH) | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | – | – | 1.20 | – | – | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.22 | – | 0.38 | 0.009 | – | 0.015 |
| b1 | 0.22 | 0.30 | 0.33 | 0.009 | 0.012 | 0.013 |
| c | 0.12 | – | 0.21 | 0.005 | – | 0.008 |
| c1 | 0.10 | 0.127 | 0.16 | 0.004 | 0.005 | 0.006 |
| D | 22.22 BSC | | | 0.875 BSC | | |
| ZD | 0.71 REF | | | 0.028 REF | | |
| E | 11.76 BSC | | | 0.463 BSC | | |
| E1 | 10.16 BSC | | | 0.400 BSC | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.80 REF | | | 0.031 REF | | |
| e | 0.65 BSC | | | 0.026 BSC △8 | | |
| R1 | 0.12 | – | – | 0.005 | – | – |
| R2 | 0.12 | – | 0.25 | 0.005 | – | 0.010 |
| θ | 0° | – | 8° | 0° | – | 8° |
| θ1 | 0° | – | – | 0° | – | – |
| θ2 | 10° | 15° | 20° | 10° | 15° | 20° |
| θ3 | 10° | 15° | 20° | 10° | 15° | 20° |

NOTE:

1. DATUM PLANE -H- COINCIDENT WITH BOTTOM OF LEAD. WHERE LEAD EXITS BODY.
2. TO BE DETERMINED AT SEATING PLANE -C- .
3. DIMENSION D AND E1 ARE DETERMINED AT DATUM -H- .
   DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. REFER TO JEDEC STD MS–024, FC. △8

PART NUMBERING SYSTEM

| AS4C | 64M16D1 | 6 | T | C/I | N |
|---|---|---|---|---|---|
| DRAM | 64M16=64Mx16<br>D1=DDR1 | 6= 166MHz | T = TSOP II | C=Commercial<br>(0° C- +85° C)<br>I=Industrial<br>(-40° C- +85° C) | Indicates Pb and Halogen Free |

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