

AS4C1G8MD3LA-10BIN vs IM8G08D3FDDG-125I Comparison

Part Number & result Parameter	AS4C1G8MD3LA-10BIN	IM8G08D3FDDG-125I	Comparison Result
Product Description	DDR3L SDRAM	DDR3L SDRAM	Same
Density/Memory Size	8Gb	8Gb	Same
Memory Organization	128Meg x 8 x 8 banks	128Meg x 8 x 8 banks	Same
Data Bus Width	8 bits	8 bits	Same
Row Address	64K (A[15:0])	64K (A[15:0])	Same
Column Address	2K (A[11,9:0])	2K (A[11,9:0])	Same
Page Size	2KB	2KB	Same
Operating Power Supply	VDD/Q=1.35V (1.283~1.45V)	VDD/Q=1.35V (1.283~1.45V)	Same
DDR3 Compatibility	Yes (VDD/Q= 1.425V ~1.575V)	Yes (VDD/Q= 1.425V ~1.575V)	Same
Operating Temperature	Industrial (-40°C ≤ Tc ≤ +95°C)	Industrial (-40°C ≤ Tc ≤ +95°C)	Same
Max. Clock Frequency	933 MHz	800 MHz	Alliance faster
Max Data Rate (MT/s)	1866 Mbps	1600 Mbps	Alliance faster
tRCD/tRP/CL	13.91/13.91/13 for 933Mhz 13.75/13.75/11 for 800Mhz	13.75/13.75/11	Comparable
Die per Package	Dual Die Part	Dual Die Part with Dual control pins	Different
Package	78b FBGA (9mm x 10.6mm)	78b FBGA (9mm x 10.6mm)	Same
Package Material	Pb and Halogen Free	Pb and Halogen Free	Same
Pin to Pin Compatible Register settings	Single "CS", "CKE", "ODT" & "ZQ" pins	Dual "CS", "CKE", "ODT" & "ZQ" pins	Different

AS4C1G8D3LA
78-ball FBGA (x8 configuration)

	1	2	3	4	5	6	7	8	9
A	V _{SS}	V _{DD}	NC	NC	V _{SS}	V _{DD}	NC	V _{SS}	V _{DD}
B	V _{SS}	V _{SSQ}	DQ0	DM	V _{SSQ}	V _{DDQ}	V _{SSQ}	V _{DDQ}	DQ0
C	V _{DDQ}	DQ2	DQS	DQ1	DQ3	V _{SSQ}	V _{SSQ}	V _{DDQ}	DQ2
D	V _{SSQ}	DQ6	DQS	V _{DD}	V _{SS}	V _{SSQ}	V _{SSQ}	V _{DDQ}	DQ6
E	V _{REFDQ}	V _{DDQ}	DQ4	DQ7	DQ5	V _{DDQ}	V _{DDQ}	V _{SSQ}	DQ4
F	NC	V _{SS}	RAS	CK	V _{SS}	NC	CK	V _{SS}	RAS
G	ODT	V _{DD}	CAS	CK	V _{DD}	CAS	CK	V _{DD}	CAS
H	NC	CS	WE	A10/AP	ZQ	NC	A10/AP	ZQ	NC
J	V _{SS}	BA0	BA2	A15	V _{REFCA}	V _{SS}	A15	V _{REFCA}	V _{SS}
K	V _{DD}	A3	A0	A12/BC	BA1	V _{DD}	A12/BC	BA1	V _{DD}
L	V _{SS}	A5	A2	A1	A4	V _{SS}	A1	A4	V _{SS}
M	V _{DD}	A7	A9	A11	A6	V _{DD}	A11	A6	V _{DD}
N	V _{SS}	RESET	A13	A14	A8	V _{SS}	A14	A8	V _{SS}

IM8G08D3FDDG-125I
78-ball FBGA (x8 configuration)


	1	2	3	4	5	6	7	8	9
A	V _{SS}	V _{DD}	NC	NC	V _{SS}	V _{DD}	NC	V _{SS}	V _{DD}
B	V _{SS}	V _{SSQ}	DQ0	DM	V _{SSQ}	V _{DDQ}	V _{SSQ}	V _{DDQ}	DQ0
C	V _{DDQ}	DQ2	DQS	DQ1	DQ3	V _{SSQ}	V _{SSQ}	V _{DDQ}	DQ2
D	V _{SSQ}	DQ6	DQS	V _{DD}	V _{SS}	V _{SSQ}	V _{SSQ}	V _{DDQ}	DQ6
E	V _{REFDQ}	V _{DDQ}	DQ4	DQ7	DQ5	V _{DDQ}	V _{DDQ}	V _{SSQ}	DQ4
F	ODT1	V _{SS}	RAS	CK	V _{SS}	CKE1	CK	V _{SS}	RAS
G	ODT0	V _{DD}	CAS	CK	V _{DD}	CAS	CK	V _{DD}	CAS
H	CS1	CS0	WE	A10/AP	ZQ0	ZQ1	A10/AP	ZQ0	ZQ1
J	V _{SS}	BA0	BA2	A15	V _{REFCA}	V _{SS}	A15	V _{REFCA}	V _{SS}
K	V _{DD}	A3	A0	A12/BC	BA1	V _{DD}	A12/BC	BA1	V _{DD}
L	V _{SS}	A5	A2	A1	A4	V _{SS}	A1	A4	V _{SS}
M	V _{DD}	A7	A9	A11	A6	V _{DD}	A11	A6	V _{DD}
N	V _{SS}	RESET	A13	A14	A8	V _{SS}	A14	A8	V _{SS}