

# Reliability Qualification Report

for

**LPDDR4X SDRAM with Pb/Halogen Free  
(Industrial)**

**(8Gb ,512M×16,AS4C512M16MD4VA-046BIN)**

## 2. General Information

Part Number	Density / Operating Condition				PKG	Qualification
	Density Org.	Max. Clock Freq.	Temperature	Voltage		
AS4C512M16MD4 VA-046BIN	8Gb X16	2133MHZ	-40°C to +85°C	VDD1=1.8V, VDD2=1.1V, VDDQ=0.6V	200ball FBGA	Qualified

### 3. Accelerated Test Results

#### -. Life Test Results for 8Gb LPDDR4x SDRAM

Reliability item	Ref	Condition	Samples	Test Results (No. of Fail)			
				48 hrs	168 hrs	504 hrs	1008 hrs
EFR (Early Life Failure Rate)	AEC Q100-008 JESD22-A108	Dynamic Stress Ta=125°C	2,000	0	-	-	-
HTOL (High Temperature Operating Life)	JESD22-A108	Dynamic Stress Ta=125°C	387	-	0	0	0
MTTF of EFR and HTOL				338.6 ppm	57.07FIT	19.02FIT	9.51FIT
LTOL (Low Temperature Operating Life)	JESD22-A108	Dynamic Stress Ta=125°C	387	-	0	0	0

$$AFv = \exp\{\beta \cdot (V_{\text{stress}} - V_{\text{use}})\}$$

- AFv : Voltage acceleration factor
- Vuse : Internal voltage at normal use
- Vstress : Internal voltage at EFR, HTOL
- $\beta$  : Constant (dependent upon electric field constant, oxide thickness, etc)  
 $\beta = 8/V$ . And then **EFR & HTOL AFv=11.02**

**$A_{ft} = \exp\{E_a/K \cdot (1/T_{a\_use} - 1/T_{a\_stress})\}$**

- $A_t$  : Temperature acceleration factor
  - $E_a$  : Activation energy
  - $T_{a\_use}$  : Ambient temperature (in K) at  $T_a = 55^\circ\text{C}$  (Temperature at normal use)
  - $T_{a\_stress}$  : Ambient temperature (in K) (Temperature at EFR, HTOL)
  - $K$  : Boltzman's constant =  $8.623 \times 10^{-5}$  eV/K
- $T_{use} = 55^\circ\text{C}$ ,  $T_{stress} = 125^\circ\text{C}$ ,  $E_a = 0.5\text{V}$ , And then **EFR & HTOL  $A_{ft} = 22.40$**

**$AF = A_{fv} * A_{ft} = 11.02 * 22.40 = 246.96$**

## 4. Electrical Verification Test Results

### -. ESD and Latch up for 8Gb LPDDR4x SDRAM

Reliability item	Test Standard	Condition	Sample	Criteria	Test Results
Electro Static Discharge	AEC Q100-002 MIL-STD-883	HBM	3 per condition	1,000V	Pass (> 1,500V)
	JESD22-A115B	MM	3 per condition	200V	Pass (> 500V)
Latch-Up	AEC Q100-004 JESD78	Vcc Test @85°C	3 per condition	$\geq 1.5 \times V_{cc.max}$	Pass (>2.93V)
		I Test @ 85°C	3 per condition	$\geq \pm 150mA$	Pass (>150mA)

## 5. Environmental Stress Test Results

Reliability item	Ref.	Condition	Sample	Test Results (No. of Fail)		
PC (Preconditioning, MSL3)	J-STD-020 JESD22-A113	Temp. cycle(-50°C/150°C, 5cycle)+Baking 125°C/24Hrs +Soak (30°C/60%RH,192hrs) +IR Reflow(250°C, 3 times)	270	0		
					168hrs	504hrs
HTSL (High Temperature Storage Life Test)	JESD22-A103	Ta=150°C	135	0	0	0
					48hrs	96hrs
Biased HAST* (Highly Accelerated Temperature and Humidity Stress Test)	JESD22-A110	Ta=130°C, R.H=85%, VDD = 1.9 5 V, VBB= 0.65 V, VCC = 1.17 V, VREF= 1.17 V	135	0	0	
					200cyc	500cyc
TC* (Temperature Cycle)	JESD22-A104	-25°C/+125°C air to air	135	0	0	0

❖ PC performed before HAST and TC stresses.

## 6. Fab. Process Reliability Test Results

Item	Sample Size	Test Condition	Test Results (0.1% Fail Time)	Failure Criteria
TDDB	3Wafer / 3Lot	Bias : 5.6V / 5.8V / 6.0V Temp. : 125°C	> 10years	F(100Khr) < 0.01% Fail
Hot Carrier	3Wafer / 3Lot	Vg : Vg at max Isub Vd : 3.7V / 3.9V / 4.1V	> 10years	F(100Khr) < 0.1% Fail ( $\Delta I_{DSat} > 10\%$ )
NBTI	3Wafer / 3Lot	Bias : 2.1V/1.9V/1.7V Temp. : 125°C	> 10years	F(100Khr) < 0.1% Fail ( $\Delta I_{DSat} > 10\%$ )
E/M	3Wafer / 3Lot	Current Density : 2~7 MA/Cm2 Temp. : 200~300°C	> 10years	F(100Khr) < 0.1% Fail ( $\Delta R > 10\%$ )
S/M	3Wafer / 3Lot	Temp. : 250°C	> 10years	F(100Khr) < 0.1% Fail ( $\Delta R > 5\%$ )

## 7. Soft Error Rate for DRAM

### - High Energy Neutron Test for 8Gb LP DDR4x

<b>Test Site</b>	<b>TRIUMF@CANADA</b>					
<b>Beam type</b>	<b>Neutron</b>					
<b>Sample Size</b>	<b>4 pcs</b>					
<b>Overall Test Results</b>	<b>SBU</b>	<b>MBU</b>	<b>SEL</b>	<b>SEFI</b>		
				<b>Row</b>	<b>Col</b>	<b>Total</b>
<b>FIT / Gbit</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0.031</b>	<b>0.265</b>	<b>0.296</b>

- The overall cosmic-ray FIT at sea level in NYC

- $\text{FIT/Chip} = \text{FIT/Gbit} * \text{Chip Density[Gbit]}$

\* SBU(Single Bit Upset), MBU(Multiple Bit Upset), SEL(Single Event Latch-up), SEFI(Single Event Functional Interrupt)