Reliability Qualification Report

for

DDR2 SDRAM with Pb/Halogen Free

(38nm 1Gb DDR2 SDRAM AS4C64M16D2B-25BCN)

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1. Information

Product	1Gb DDR2 SDRAM
Device	AS4C64M16D2B-25BCN
Technology	38nm
Function	64M*16 DDRII

Package Type	84B FBGA
Leadframe/ Substrate	BT
Lead Finish	Sn/Ag/Cu 96.5/3/0.5 ; 0.45mm
Molding Compound	HITACHI CEL-1702HF
Package Size	8*10.5 / 8*12.5 mm^2

2. Life Test

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
2.1 High Temperature Operation Life Test *	Ta = 125 ℃; VDD > 1.9V	231	168hrs 500hrs 1000hrs	0/231 0/231 0/231
2.2 Low Temperature Operation Life Test *	Ta = -45 ℃; VDD > 1.9V	120	168hrs 500hrs 1000hrs	0/120 0/120 0/120

Remark:

*. Preconditioning : J-STD-020 (MSL-2)
Baking @ 125℃ , 24 hours. => Soaking @ 85℃ / 60% R.H., 168 hours => IR : 3 times,

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
2.3 Early Life Test	Ta = 125 ℃; VDD > 1.9V	9,600	48hrs	8/9600

3. Environmental Test

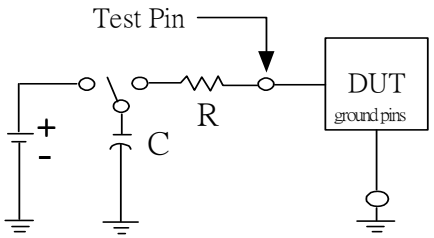
Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
3.1 High Temperature Storage Life Test *	Ta. = 150℃	231	168hrs 500hrs 1000hrs	0/231 0/231 0/231
3.2 Temperature Cycle Test *	Ta.= -65℃ / +150℃	231	500cycs	0/231
3.3 Autoclave (AC)	Ta. = 121℃/ 100%RH;	231	192hrs	0/231
3.4 Highly Accelerated Temperature and Humidity Stress *	Ta. = 110℃/ 85%RH; VDD = 1.9V	231	264hrs	0/231

Remark:

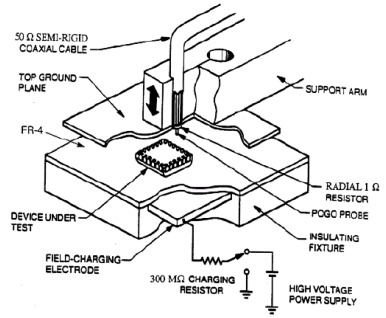
*. Preconditioning : J-STD-020 (MSL-2)
Baking @ 125℃ , 24 hours. => Soaking @ 85℃ / 60% R.H., 168 hours => IR : 3 times,

4. ESD Test

4.1 a. Human Body Model (HBM) Test Circuit



b. Charge Device Model (CDM) test circuit:



* Human Body Model (HBM)

◦ Stress Voltage : ±2000V

◦ Sample size : 10 ea/ lot, total 3 lots

Charge Device Model (CDM)

◦ Stress Voltage : ±1000V

◦ Sample size : 6 ea/ lot, total 3 lots

4.2 Reference: HBM: JS-001; AEC Q100-002
CDM: JESD22-C101, AEC Q100-011

4.3 Judgment Criteria : Pass Leakage, standby current and functionality tests at both high and low temperature.

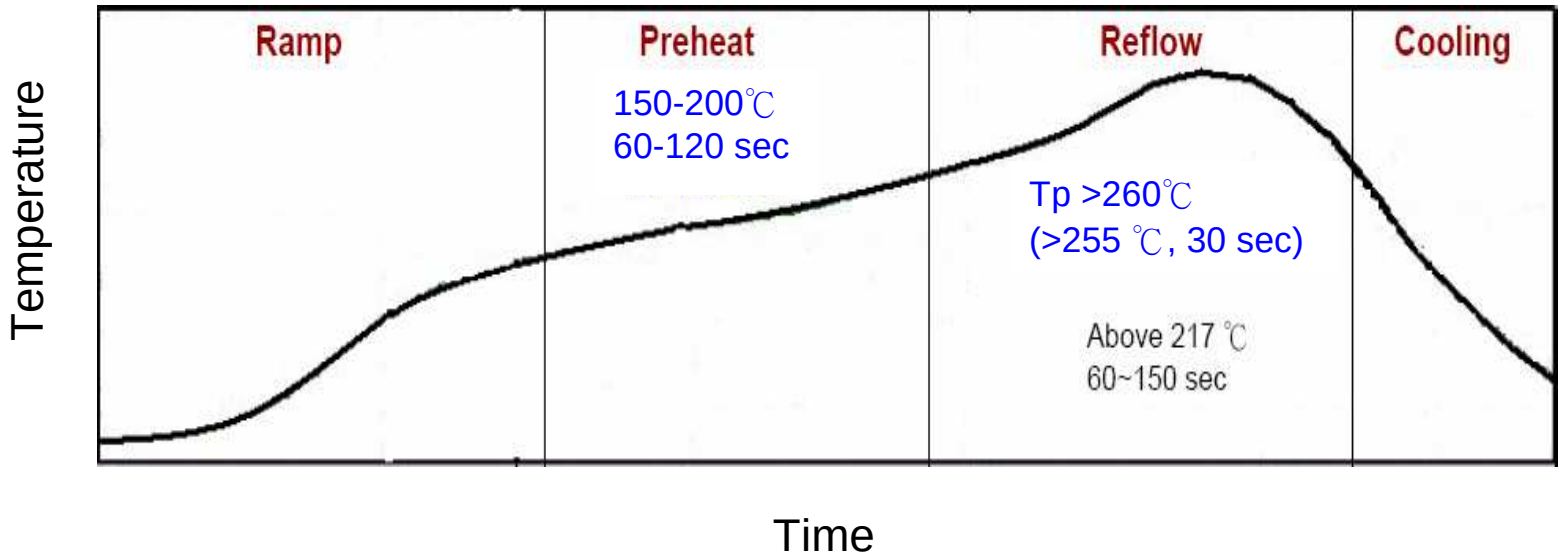
4.4 Test Result : **HBM : > ±2000V**
CDM : > ±1000V

5. Latch-up Test

Test Items	Test Conditions	Sample Size	Results (Number of failures)
5.1 I-test	>±200mA ; Ta = 95 ℃	12 ea/lot, 3 lots	0/36
5.2 V-supply over voltage test	+1.5xVddMAX ; Ta = 95 ℃	6 ea/lot, 3 lots	0/18

5.3 Reference: JESD78A, AEC Q100-004

6. IR-reflow Profile



1. The IR reflow profile follows the IPC/JEDEC J-STD-020D.1.
2. Ramp up rate: 3 ℃/sec max., Ramp down rate: 6 ℃/sec max..
3. The maximum temperature should be limited to 260 ℃.
4. Time above liquidus temperature (217 ℃) should be 60~150 sec.
5. The re-flow should not be repeated for more than 3 times.
6. Time 25 °C to peak temperature should be 8 minutes maximum.