Reliability Qualification Report

for

DDRIIIL SDRAM with Pb/Halogen Free

(64M×16, DDR3 SDRAM AS4C64M16D3LW-10BCN)

Issued Date: Aug 1, 2025

SUMMARY

AS4C64M16D3LW , Package type- 96 VFBGA passed all commercial grade temperature (0~95C) qualification tests according to Alliance`s product qualification requirement. A summary of the test result is as follows :

- ▲ . **Pre-condition Test : 0/1500 pcs**
- ▲ . **High Temp. Operating Life test : 0/231 pcs**
- ▲ . **High Temp. Storage Life Test : 0/231 pcs**
- ▲ . **Highly Accelerated Stress Test : 0/231 pcs**
- ▲ . **Temperature Cycle Test : 0/231 pcs**
- ▲ . **Un-bias Highly Accelerated Stress Test : 0/231 pcs**
- ▲ . **ESD-HBM : 0/72 pcs**
- ▲ **ESD-CDM : 0/9 pcs**
- ▲ . **Latch -Up Test : 0/18 pcs**

Results of the life tests and environmental tests as well as the methods used on **AS4C64M16D3LW** DDR3 SDRAM are described in details in the report.

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Ⅰ. PRODUCT DESCRIPTION

FEATURES

- Power Supply: V_{DD}, V_{DDQ} = 1.5V ± 0.075V
- Double Data Rate architecture: two data transfers per clock cycle
- Eight internal banks for concurrent operation
- 8 bit prefetch architecture
- CAS Latency: 6, 7, 8, 9, 10, 11, 13 and 14
- Burst length 8 (BL8) and burst chop 4 (BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or nibble sequential
- Bi-directional, differential data strobes (DQS and DQS#) are transmitted / received with data
- Edge-aligned with read data and center-aligned with write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge, data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- Posted CAS with programmable additive latency (AL = 0, CL - 1 and CL - 2) for improved command, address and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Auto-precharge operation for read and write bursts
- Refresh, Self-Refresh, Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Precharged Power Down and Active Power Down
- Data masks (DM) for write data
- Programmable CAS Write Latency (CWL) per operating frequency
- Write Latency WL = AL + CWL
- Multi purpose register (MPR) for readout a predefined system timing calibration bit sequence
- System level timing calibration support via write leveling and MPR read pattern
- ZQ Calibration for output driver and ODT using external reference resistor to ground
- Asynchronous RESET# pin for Power-up initialization sequence and reset function
- Programmable on-die termination (ODT) for data, data mask and differential strobe pairs
- Dynamic ODT mode for improved signal integrity and preselectable termination impedances during writes

- 2K Byte page size
- Interface: SSTL_15
- Packaged in VFBGA 96 Ball (7.5x13 mm^2 with thickness of 1.0 mm), using lead free materials with RoHS compliant

GENERAL DESCRIPTION

The AS4C64M16D3LW is a 1G bits DDR3 SDRAM, organized as 8,388,608 words x 8 banks x 16 bits. This device achieves high speed transfer rates up to 1866 MT/s(DDR3-1866) for various applications. This device is sorted into the following speed grades:-10,-12,-15.

The -10 speed grades are compliant to the DDR3-1866 (13-13-13) specification which is guaranteed to support 0°C ≤ TCASE ≤ 95°C.

The -12 speed grades are compliant to the DDR3-1600 (11-11-11) specification which is guaranteed to support 0°C ≤ TCASE ≤ 95°C.

The -15 speed grades are compliant to the DDR3-1333 (9-9-9) specification which is guaranteed to support 0°C ≤ TCASE ≤ 95°C.

The AS4C64M16D3LW is designed to comply with the following key DDR3 SDRAM features such as posted CAS#,programmable CAS# Write Latency (CWL), 2Q calibration, on die termination and asynchronous reset. All of the control and address inputs are synchronized with a pair of externallysupplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising andCK# falling). All I/Os are synchronized with a differential DQS-DQS# pair in a source synchronousfashion.

Ⅱ. LIFE TEST

A. Introduction

1. Pre-condition Test

1.1 SCOPE

Pre-condition Test is to measure the resistance of SMD(Surface Mount Devices) to the storage environment at the customer site and to thermal stress created by IR reflow or Vapor Phase Reflow.

1.2 TEST CONDITION

Step 1 : TCT(-65°C/150°C, 5 cycles)
Step 2 : Bake(125°C, 24 hours)
Step 3 : Soak(60°C/60%RH, 52 hours)
Step 4 : IR (260 °C), 3 Passes.
(JEDEC 020D)

2. High Temperature Operating Life Test (HTOL)

2.1 SCOPE

HTOL test is performed to accelerate failure mechanisms, which are thermally activated. This can be achieved by stressing the devices with bias at high temperature.

All parts must be preconditioned before testing.

2.2 TEST CONDITION

Temp ambient = 125°C, Vdd = 1.575V, dynamic stressing, Td = 1000 hrs.

(JEDEC JESD-22-A108)

3. High Temperature Storage Life Test (HTSL)

3.1 SCOPE

HTSL test is to determine the stability of the device in high temperature environment.

All parts must be preconditioned before testing.

3.2 TEST CONDITION

Temp = 150°C, Td = 1000 hrs. (JEDEC JESD-22-A103)

B. Test Results

1. Pre-condtion Test

1.1 SUMMARY TABLE

Run	Lot No	Result	Remark
#1	6650A32CBZY	0/500	**Pass**
#2	665102100ZX	0/500	**Pass**
#3	665105400ZY	0/500	**Pass**

*Criteria : Acc/Rej = 0/1.

2. High Temperature Operating Life Test (HTOL)

2.1 SUMMARY TABLE

RUN	Lot No	500 Hrs	1000 Hrs	Remark
#1	6650A32CBZY	0/77	0/77	**Pass**
#2	665102100ZX	0/77	0/77	**Pass**
#3	665105400ZY	0/77	0/77	**Pass**

*Criteria : Acc/Rej = 0/1.

2.2 FAILURE RATE CALCULATION

$$F.R.(T) = \frac{X^2(1-CL, 2N+2)}{2EDH}$$

WHERE X^2: CHI-SQUARE Function CL : Confidence Level

N : No of Failures EDH : Equivalent Device Hour

Test Item	Dev. Hours at Tj=127.4°C,	Equiv. Dev. Hours at Tj=60°C,	No. of Failure	Failure Rate at 60°C
HTOL	231000	25245608	0	36.3 FIT

Based on CL = 60% and Activation Energy = 0.8 eV

3. High Temperature Storage Life Test (HTSL)

3.1 SUMMARY TABLE

Run	Lot No	500 Hrs	1000 Hrs	Remark
#1	6650A32CBZY	0/77	0/77	**Pass**
#2	665102100ZX	0/77	0/77	**Pass**
#3	665105400ZY	0/77	0/77	**Pass**

*Criteria : Acc/Rej = 0/1.

III. ENVIRONMENTAL TESTS

A. Introduction

1. Highly Accelerated Stress Testing (HAST)

1.1 SCOPE

HAST is to evaluate the reliability of non hermetic packaged solid-state device in humid environments.

All parts must be preconditioned before testing.

1.2 TEST CONDITION

Ta = 121°C, Vdd=1.575V, RH% = 85%, Td = 168 Hrs. (JESD22-A110)

2. Temperature Cycle Test (TCT)

2.1 SCOPE

TCT is to evaluate the resistance of device to environmental temperature change.

All parts must be preconditioned before testing.

2.2 TEST CONDITION

-65°C / 15min, transfer time 1min, +150 °C/15min, 500 cycles.
(JEDEC JESD-22-A104)

3. Un-bias Highly Accelerated Stress Test (UHAST)

3.1 SCOPE

UHAST is to evaluate the reliability of BGA package type product's resistance against high temperature and high humidity.

All parts must be preconditioned before testing.

3.2 TEST CONDITION

Ta = 130°C, RH% = 85%, Td = 96 Hrs. (JESD22-A118)

B. Test Results

1. Highly Accelerated Stress Testing (HAST)

1.1 SUMMARY TABLE

Run	Lot No	168 Hrs	Remark
#1	6650A32CBZY	0/77	Pass
#2	665102100ZX	0/77	Pass
#3	665105400ZY	0/77	Pass

*Criteria : Acc/Rej = 0/1.

2. Temperature Cycle Test (TCT)

2.1 SUMMARY TABLE

Run	Lot No	500 Cycles	Remark
#1	6650A32CBZY	0/77	Pass
#2	665102100ZX	0/77	Pass
#3	665105400ZY	0/77	Pass

*Criteria : Acc/Rej = 0/1.

3. Un-bias Highly Accelerated Stress Test (UHAST)

3.1 SUMMARY TABLE

Run	Lot No	96 Hrs	Remark
#1	6650A32CBZY	0/77	Pass
#2	665102100ZX	0/77	Pass
#3	665105400ZY	0/77	Pass

*Criteria : Acc/Rej = 0/1.

IV. ESD AND LATCH-UP

A. Introduction

1. ESD

1.1 SCOPE

ESD test is to evaluate the immunity of device to electrostatic discharge.

1.2 TEST CONDITION

Human Body Model (HBM) : JS-001

Charged Device Model (CDM) : JESD22-C101-C

2. Latch-Up

2.1 SCOPE

Latch-Up test is to evaluate the immunity of the devices to latch-up.

2.2 TEST CONDITION

JEDEC STD 78, Temp = 25 °C, VDD = Max. Operating Voltage

B. Test Results

1. ESD

1.1 Human Body Model

Run	LOT#	POSITIVE	NEGATIVE	Remark
#1	6650A32CBZY	0/12	0/12	**Pass**
#2	665102100ZX	0/12	0/12	**Pass**
#3	665105400ZY	0/12	0/12	**Pass**

*Criteria : Acc/Rej = 0/1.

*| SPEC | : >2 KV

1.2 Charged Device Model

Run	LOT#	POSITIVE/ NEGATIVE	Remark
#1	6650A32CBZY	0/3	**Pass**
#2	665102100ZX	0/3	**Pass**
#3	665105400ZY	0/3	**Pass**

*Criteria : Acc/Rej = 0/1.

*| SPEC | : >750V

2. Latch-Up

Run	LOT#	POSITIVE	NEGATIVE	Remark
#1	6650A32CBZY	0/3	0/3	**Pass**
#2	665102100ZX	0/3	0/3	**Pass**
#3	665105400ZY	0/3	0/3	**Pass**

*Criteria : Acc/Rej = 0/1.

*| SPEC. | : I-Test > 200mA

Vsupply over voltage Test > 1.5x max supply voltage