Reliability Qualification Report

for

ASFC16G31TA-51BCN with Pb/Halogen Free

(Embedded Multi-Media Card (e.MMC))

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0. RELIABILITY TEST SUMMARY

Test Item	Test Condition	Pass Criteria	Test Result
EFR	125°C, Vmax, 168Hrs	0/1 (A/R)	0/1000 (PASS)
OLT	125°C, Vmax, 1000Hrs	0/1 (A/R)	0/231 (PASS)
MSLT*	Level III	0/1 (A/R)	0/270 (PASS)
HTST	150℃, 1000Hrs	0/1 (A/R)	0/135 (PASS)
TCT	-65℃ ~ +150℃, 500Cycles	0/1 (A/R)	0/135 (PASS)
HAST	110℃, 85%R.H., Vmax, 264Hrs	0/1 (A/R)	0/135 (PASS)
ESD	HBM: R=1.5KΩ, C=100pF	≧±1KV	0/3 (PASS)
	CDM: Non-Socket Mode	≧±250V	0/3 (PASS)
Latch-Up	Vtr(+)≧1.5 * Vmax Itr(+)≧100mA Itr(-)≦-100mA		0/6 (PASS)

***Moisture Sensitivity Level Test Flow & Condition:**
Electrical Test → SAT → TC (-65℃~+150℃, 5Cycles) → Bake (125℃, 24Hrs) → Soak Level III (60℃, 60%R.H., 40Hrs) → Convection Reflow (260 +5/-0℃, 0~20Secs, 3Cycles) → Electrical Test → SAT

1. INTRODUCTION

In order to meet the most stringent market demands for high quality and reliability semiconductor components, Alliance maintains a strict reliability program in all products. The purpose of this report is to give an overview of the reliability status of ASFC16G31TA-51BCN. Accelerated tests are performed on product, and then the results are extrapolated to standard operating conditions in order to calculate and estimate the component's failure rate.

2. PRODUCT INFORMATION

The e.MMC products follow the JEDEC e.MMC 5.1 standards. It is an ideal universal storage solution for many electronic devices, including smart phones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. The e.MMC encloses the TLC NAND and e.MMC controller inside as one JEDEC standard package, providing a standard interface to the host. The e.MMC controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing. The ASFC16G31TA-51BCN is packaged in a standard BGA 153B.

3. RELIABILITY

Many stress tests have been standardized in such documents as MIL-STD-883, EIAJ-IC-121, EIA/JESD22 and JEDEC-NOTE-17. From these standards, Alliance has selected a series of tests to ensure that reliability targets are being met. These tests, including environmental test, ESD test and latch-up test, are discussed in the following sections.

3.1. Sample Preparation Flow

Assembly BGA 153B → FT → Sampling Good Parts for Reliability Test

3.2. Life Test

The purpose of the Early Failure Rate (EFR) and Operating Life Test (OLT) is to determine the reliability of products by accelerating thermally activated failure mechanisms by subjecting samples to extreme temperatures under biased operating condition of Vmax. The test samples are screened directly after final electrical testing.

3.2.1. Test Flow

(1) EFR Test Flow

B/I 168Hrs (125°C, Vmax) → Electrical Test

(2) OLT Test Flow

B/I 168Hrs (125°C, Vmax) → Electrical Test
→ B/I 500Hrs (125°C, Vmax) → Electrical Test
→ B/I 1000Hrs (125°C, Vmax) → Electrical Test

3.2.2. Test Criteria

Test Item	Reference Standard	Test Condition	Pass Criteria
EFR 168Hrs	JESD22-A108	Tj= 125°C Vdd= Vmax	0/1 (A/R)
OLT 1000Hrs			

3.2.3. Test Result

The life test is performed for the purpose of accelerating the probable electrical and physical weakness of devices subjected to the specified conditions over an extended time period. Table 1 and 2 shows that there is no any failure in the final result.

Test Item	Sample	Test Result (Failure / Sample Size)	Failure Mode
		168 Hrs	
EFR	1000ea	0/1000	N/A

Table 1. EFR Test Result

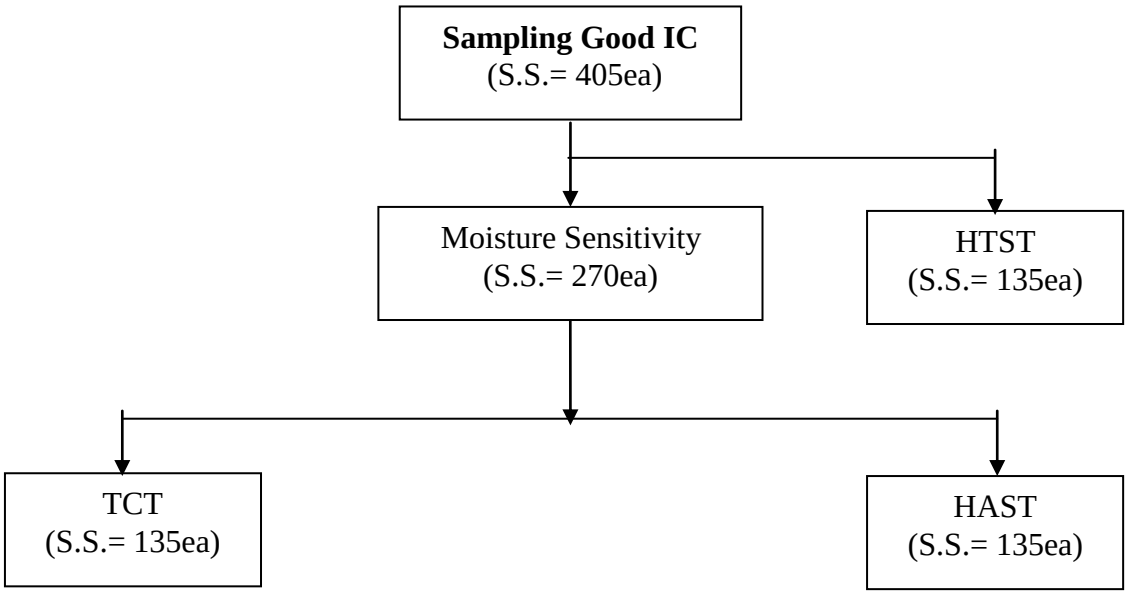
Test Item	Sample	Test Result (Failure / Sample Size)			Failure Mode
		168 Hrs	500 Hrs	1000 Hrs	
OLT	231ea	0/231	0231	0/231	N/A

Table 2. OLT Test Result

3.3. Environmental Test

The purpose of environmental test is to evaluate the ability of semiconductor device to withstand the temperature stress, humidity stress, electrical stress or any combination of these. It can reveal not only the package quality issue but also the possible error in wafer process or chip design interacting with the assembly process.

3.3.1. Test Flow



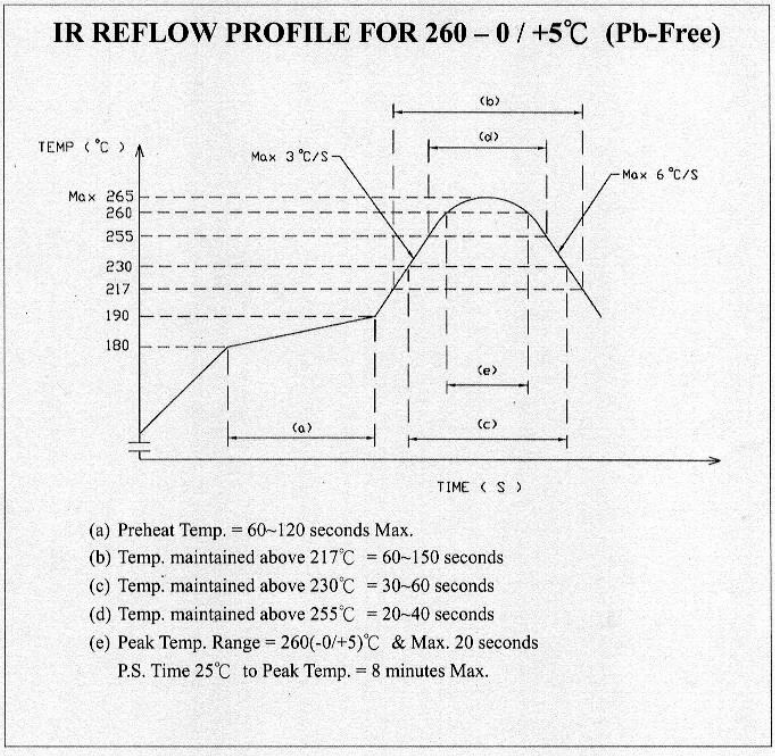
3.3.2. Test Condition and Time

3.3.2.1. Moisture Sensitivity Test

The purpose of moisture sensitivity test is to identify the classification level of nonhermetic solid state Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation.

***Moisture Sensitivity Test Flow**

Electrical Test → SAT → TC (-65℃~+150℃, 5Cycles) → Bake (125℃, 24Hrs) → Soak Level III (60℃, 60%R.H., 40Hrs) → Convection Reflow (260 +5/-0℃, 0~20Secs, 3Cycles) → Electrical Test → SAT

Test Item	Test Condition (Level III)	Test Time
Temp. Cycle	-65℃ ~ +150℃	5Cycles
Bake	125℃	24Hrs
Unbiased Temp-Humidity Soak	60℃, 60%R.H.	40Hrs
Convection Reflow		3Cycles

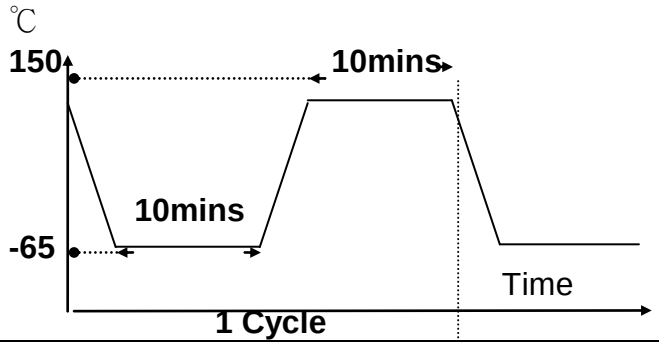
3.3.2.2. High-Temperature Storage Life Test

The high-temperature storage life test measures device resistance to a high-temperature environment that simulates a storage environment. The stress temperature is set to 150℃ in order to accelerate the effect of temperature on the test samples. In the test, no voltage bias is applied to the de-vices.

Test Item	Test Condition	Test Time
HTST	150℃	1000Hrs

3.3.2.3. Temperature Cycling Test

The purpose of temperature cycling test is to study the effect of thermal expansion mismatch among the different components within a specific die and package system. The cycling test system has a cold dwell at -65℃ and a hot dwell 150℃, and it employs a circulating air environment to ensure rapid stabilization at a specified temperature. During temperature cycling test, devices are inserted into the cycling test system and held at cold dwell for 10 minutes, and then the devices are heated to hot dwell for 10 minutes. One cycle includes the duration at both extreme temperatures and the two transition times. The transition period is less than one minute at 25℃. Samples of surface mount devices must first undergo preconditioning and pass a final electrical test prior to the temperature cycling test.

Test Item	Test Condition	Test Time
TCT		500Cycles

3.3.2.4. Highly-Accelerated Temperature and Humidity Stress Test

The highly-accelerated temperature and humidity stress test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid-state device in an environment with high humidity. It employs severe condition of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductor that pass through it. The stress conditions of the HAST are 110℃, 85% relativity humidity and Vmax operating voltage. Samples of surface mount devices are subjected to preconditioning and a final electrical test prior to the highly-accelerated temperature and humidity stress test.

Test Item	Test Condition	Test Time
HAST	110℃, 85%R.H., Vmax	264Hrs

3.3.3. Test Criteria and Result

Table 3 shows the test results and reference standard of environmental test. The test status and results of ASFC16G31TA-51BCN are also presented in the table. All pass from these test results mean that Alliance‘s

products are much more endurable in most of their service environment.

Test Item	Reference Standard	A/R Criteria	Failure/S.S.	Status	Failure Mode
Moisture Sensitivity	J-STD-020	0/1	0/270	PASS	N/A
HTST	JESD22-A103	0/1	0/135	PASS	N/A
TCT*	JESD22-A104	0/1	0/135	PASS	N/A
HAST*	JESD22-A110	0/1	0/135	PASS	N/A

*** Sampling from Moisture Sensitivity**

Table 3. Environmental Test Criteria and Result

3.4. ESD Test

Electrical discharge into semiconductor product is one of the leading causes of device failure in the customer‘s manufacturing process. Alliance performs the ESD test to ensure that the performance of ASFC16G31TA-51BCN will not be degraded to an unacceptable level by exposure to a succession of electro-static discharge. The test methods and test results are shown in Table 4.

Test Item	Test Method				Result (F/S.S)
	Reference Standard	Test Condition	Criteria	Sample	
H.B.M.	JS-001	R=1.5KΩ, C=100pF	≥±1KV	3ea	0/3
C.D.M.	JS-002	Non-Socket Mode	≥±250V	3ea	0/3

Table 4. ESD Test Condition and Result

3.5. Latch-Up Test

CMOS products can be prone to over-voltage exceeding the maximum device rating if the parasitic p-n-p-n SCRs (Silicon-controlled rectifier) are improperly biased. When the SCR turns on, it draws excessive current and causes products being damaged by thermal runaway. The Table 5 shows the latch-up test method and the test result of no failure.

Test Item	Test Method			Result (F/S.S)
	Reference Standard	Test Condition & Criteria	Sample	
Latch-Up	JESD78	Vtr(+)≧1.5 * Vmax Itr(+)≧100mA Itr(-)≦-100mA	6ea	0/6

Table 5. Latch-Up test Condition and Result

4. CONCLUSION

Reliability test is to ensure the ability of a product in order to perform a required function under specific conditions for a certain period of time. Through those tests, the devices of potential failure can be screened out before shipping to the customer. At the same time, the test results are fed back to process, design and other related departments for improving product quality and reliability.

The results of environmental test, ESD test and latch-up test also ensure that the ASFC16G31TA-51BCN is manufactured under a precise control of quality work by Alliance and its subcontractors. ***Thus, this experiment based on the Alliance reliability test standard for above test items can all pass***.

With the extensive research and development activities and the cooperation of all departments, Alliance continuously sets and maintains higher standard of quality and reliability to satisfy the future demand of its customers.