Reliability Qualification Report

for

ASFC8G31MB-51BIN with Pb/Halogen Free

(Embedded Multi-Media Card (e.MMC))

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Contents

1. Test Result Summary

One lot submit to qualification tests according to Alliance's qualification plan. A summary of the test result is listed as follows.

Test Item		Criteria	Test Result
Package Level	HTOL	1000 hrs	PASS
	HTSL	1000 hrs	PASS
	Pre-condition	MSL-3	PASS
	UHAST	264 hrs	PASS
	HAST	264 hrs	PASS
	TCT	500 cycles	PASS

2. Product Description

Part Number	ASFC8G31MB-51BIN
Process	40nm LP process
Package Type	153-TFBGA (11.5x13 mm) MCMBGA
Lot No	Specified in each test item
Flash Type	SS14N064G MLC

3. Package Level

3.1 High Temperature Operating Life Test (HTOL):

3.1.1 Purpose :

The HTOL test is to evaluate the endurance of devices when they are submitted to electical stress and thermal stress over an extended time period.

3.1.2 Test Condition ; JEDEC JESD22-A108

Ambient temperature = 125 ℃

Vccmax = 1.1X Vcc

Test duration = 1000 hrs

3.1.3 Test Result : PASS

Lot No	Result	Failure Rate(λ)	MTTF(years)
NBUU13x.00	0/77	153	747.5

Criteria : Based on CL = 60% and Activation Energy = 0.7eV

Acceleration factor AF = AFT * AFV = 77.94(Tj =125℃-55℃)

Chi-Square Distribution:60% Confidence

3.2 High Temperature Storage Life Test (HTSL):

3.2.1 Test Condition : JEDEC JESD22-A103

High ambient temperature = 150 ℃

Test duration = 1000 hrs

3.2.2 Test Result : PASS

Lot No	Result	Remark
N60Q31x.xx	0/45	N/A

3.3 Pre-condition Test (MSL-3):

3.3.1 Purpose :

The pre-condition test is to measure the resistanceof SMDs (Surface Mounting Devices) to the storage environment at the customer site and to thermal stress created by IR reflow or Vapor Phase Reflow.

3.3.2 Test Condition : JEDEC JESD 22-A113

3.3.2.1 External Visual & Function Test

3.3.2.2 SAT Inspection

3.3.2.3 Temperature Cycle (-65 ℃/150 ℃, 5 cycles)

3.3.2.4 Baking (125 ℃, 24 hours)

3.3.2.5 Temp & Humidity Soaking (30℃/60% RH, 192 hours)

3.3.2.6 IR Reflow * 3

3.3.2.7 External Visual & Function Test

3.3.2.8 SAT Inspection

3.3.3 Test Result : PASS

Lot No	Result	Remark
N60Q31x.xx	0/135	N/A

Criteria : Acc/Rej = 0/1

3.4 Unbiased High Acceleration Stress Test(UHAST)

3.4.1 Purpose :

The UHAST is designed to determine the moisture resistance of devices by subjecting them to high steam pressure levels. This test is only performed on plastic/epoxy encapsulated devices and not on hermetic packages.

3.4.2 Test Condition : JEDEC JESD 22-A118

Ambient temperature = 110 ℃

Ambient humidity = 85% RH

Test duration = 264 hrs

3.4.3 Test Result : PASS

Lot No	Result	Remark
N60Q31x.xx	0/45	N/A

Criteria : Acc/Rej = 0/1

3.5 Temperature Cycling Test (TCT):

3.5.1 Purpose :

The TCT test is provided to evaluate the structural endurance of semiconductor devices when they are exposed to high and low temperature conditions, and their endurance when they are exposed to repeated temperature variation cycles from high temperature to low temperature by circulating air.

3.5.2 Test Condition : MIL-STD 883D-1010.7, JEDEC JESD22-A104

High temperature = 150 ℃

Low temperature = -65 ℃

Test duration = 500 cycles

3.5.3 Test Result : PASS

Lot No	Result	Remark
N60Q31x.xx	0/45	N/A

Criteria : Acc/Rej = 0/1

3.6 Highly Accelerated Temperature and Humidity Stress Test (HAST)

3.6.1 Purpose :

The Highly-Accelerated Temperature and Humidity Stress Test is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It employs severe conditions of temperature, humidity, and bias which accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. The stress usually activates the same failure mechanisms as the “85/85” Steady-State Humidity Life Test (JEDEC Standard No. 22-A101).

3.6.2 Test Condition : JEDEC JESD22-A110

Ambient temperature = 110 ℃

Ambient humidity = 85% RH

Test duration =264 hrs

3.6.3 Test Result : PASS

Lot No	Result	Remark
N60Q31x.xx	0/45	N/A

Criteria : Acc/Rej = 0/1

4. ESD and Latch-Up Tests:

4.1 ESD-HBM/CDM Test:

4.1.1 Purpose :

The ESD test is to evaluate the immunity of semiconductor devices against stastic electricity to which they are exposed during their handling.

4.1.2 Test Condition : MIL-STD-883 (HBM)

JEDEC JESD22-C101 (CDM)

4.1.

Model	Lot No	Result	Remark
HBM	NBUU13x.00	PASS	All test pins ≥ ±2KV
CDM	NBUU13x.00	PASS	All test pins ≥ ±500V

Criteria : Acc/Rej = 0/1

4.2 Latch-Up Test:

4.2.1 Purpose :

The latch-up test is to evaluate the immunity of semiconductor devices (mainly CMOS devices) to "latch-up" that is a temporary short-circuiting between the power source and the ground caused by electrical noise coming from I/O and power supply pins of a device through two parasitic bipolor structures before a power supply is removed.

4.2.2 Test Condition :JEDEC JESD78

4.2.3 Test Result : PASS

Test Item	Lot No	Result	Remark
Trigger Current	NBUU13x.00	PASS	≧±200mA
Over Voltage Test	NBUU13x.00	PASS	≧1.5X VCC

Trigger Criteria : Acc/Rej = 0/1, |Spec| : ≥ ±200mA

Over Voltage Test: ≧1.5X VCC

5. Recommend reflow profile for Lead free Product:

5.1 Condition:

Follow: IPC/JEDEC J-STD-020
Average ramp-up rate (217℃to peak): 3 ℃/sec. max
Preheat：150~200℃、60~120 seconds
Temperature maintained above 217℃ 60~150 seconds
Time within 5℃of actual peak temperature: 30 seconds
Peak temperature：260+0℃
Ramp-down rate: 6℃/sec. Max.
Time 25℃to peak temperature: 8 minutes max.
Cycle interval: 5 minutes