

Revision History**5V 1Mb (128K x 8) FAST Asynchronous SRAM, rev.D**

Revision	Details	Date
Rev 1.0	Initial Release	March. 2025
Rev 1.1	Added AS7C1024D-12JIN (400mils SOJ) Part	December, 2025

FEATURES

- Fast access time : 12ns
- Low power consumption:
Operating current : 50 (TYP.) Standby
current : 1mA (TYP.)
- Single 4.5V ~ 5.5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- Packages :
 - 32-pin 300mils SOJ
 - 32-pin 400mils SOJ

GENERAL DESCRIPTION

The AS7C1024D is a 1,048,576-bit Low power CMOS FAST static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

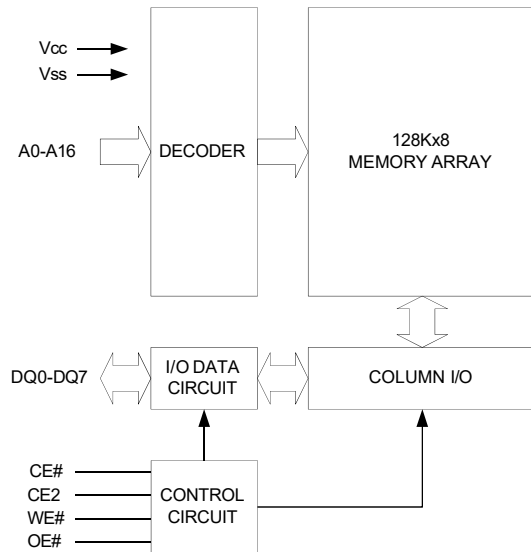
The AS7C1024D is well designed for very high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS7C1024D operates from a single power supply of 4.5V ~ 5.5V and all inputs and outputs are fully TTL compatible

ORDERING INFORMATION

Product	Package	Operating Temperature	V _{CC} Range	Speed	Power Dissipation	
					Standby (I _{SB1} , TYP.)	Operating (I _{CC} , TYP.)
AS7C1024D-12TJIN	32p SOJ (300mils)	-40 ~ 85°C	4.5 ~ 5.5V	12ns	1mA	50mA
AS7C1024D-12JIN	32p SOJ (400mils)	-40 ~ 85°C	4.5 ~ 5.5V	12ns	1mA	50mA

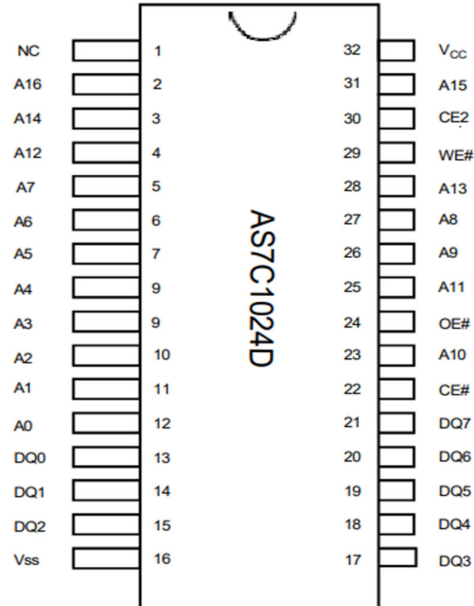
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	-40 to 85	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I_{SB}, I_{SB1}
	X	L	X	X	High-Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High-Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}		4.5	5.0	5.5	V
Input High Voltage	V _{IH} ^{*1}		2.4	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ^{*2}		- 0.5	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≧ V _{IN} ≧ V _{SS}	- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≧ V _{OUT} ≧ V _{SS} , Output Disabled	- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = MIN. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	-	50	80	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} or CE2 = V _{IL} Others at V _{IL} or V _{IH}	-	3	20	mA
	I _{SB1}	CE# ≧ V _{CC} -0.2V or CE2 ≧ 0.2V	-	1	5	mA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C1024D-12		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	12	-	ns
Address Access Time	t_{AA}	-	12	ns
Chip Enable Access Time	t_{ACE}	-	12	ns
Output Enable Access Time	t_{OE}	-	6	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	3	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	6	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	6	ns
Output Hold from Address Change	t_{OH}	3	-	ns

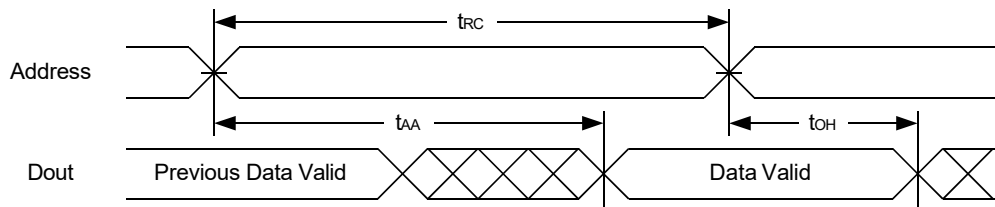
(2) WRITE CYCLE

PARAMETER	SYM.	AS7C1024D-12		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	12	-	ns
Address Valid to End of Write	t_{AW}	10	-	ns
Chip Enable to End of Write	t_{CW}	10	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	9	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	7	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	3	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	7	ns

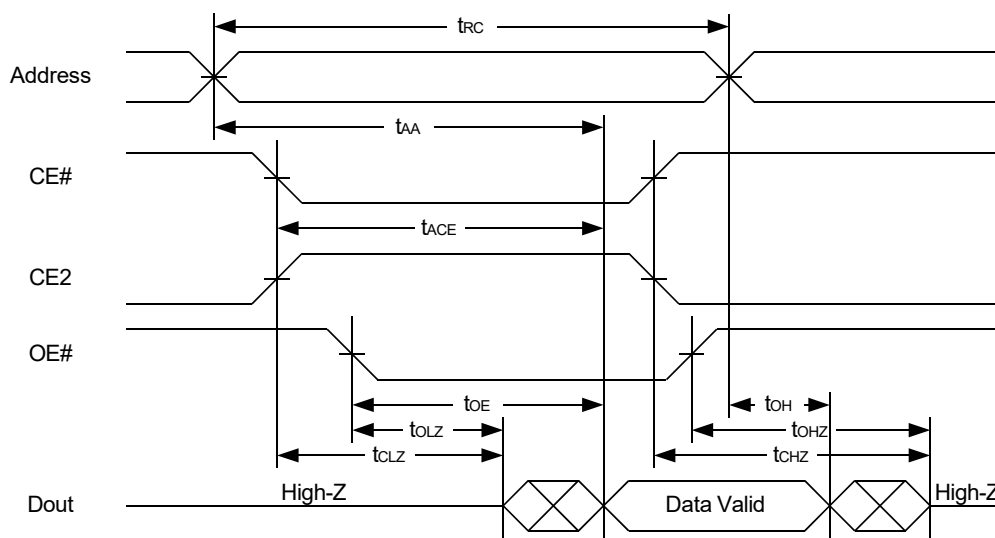
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



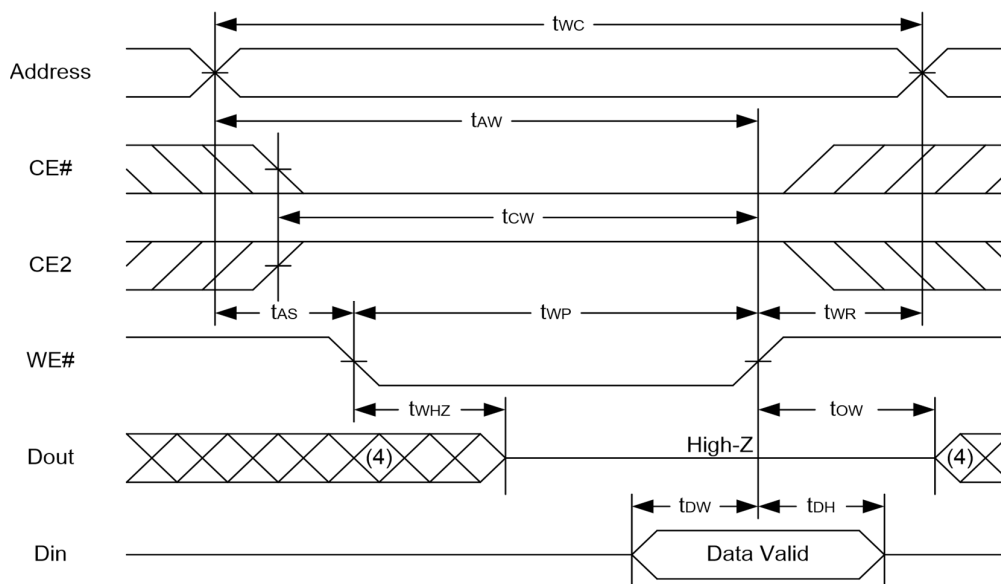
READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



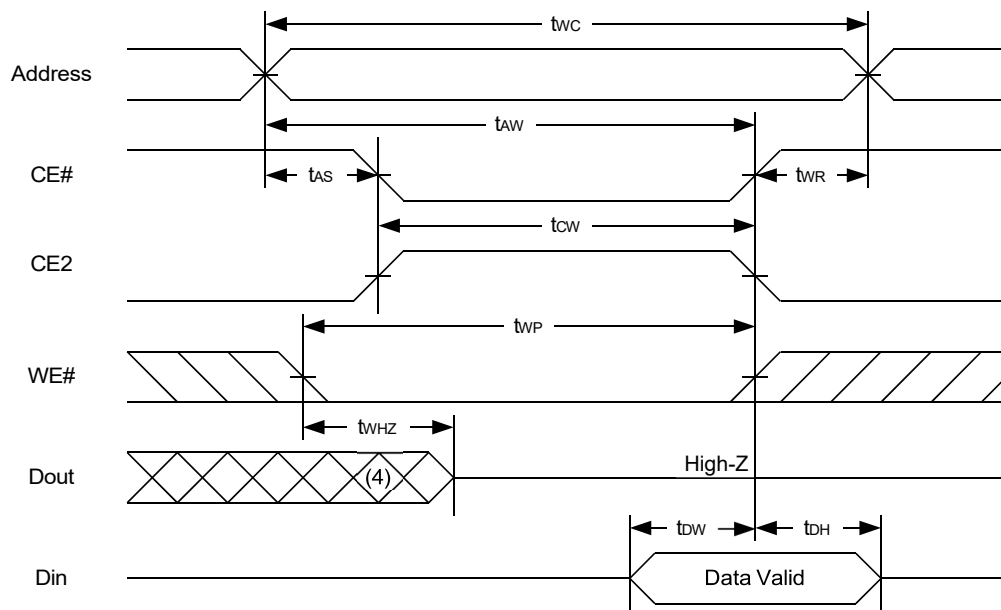
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,4,5)



Notes :

1. A write occurs during the overlap of a low CE#, high CE2, low WE#.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{OW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.

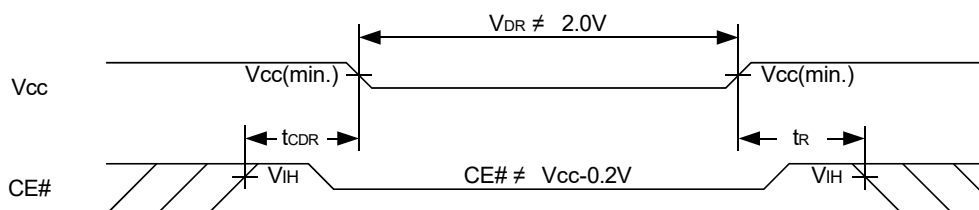
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V or CE2 $\leq$ 0.2V	-	0.01	3	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

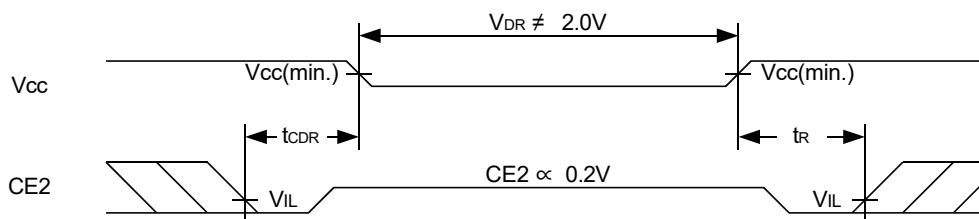
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

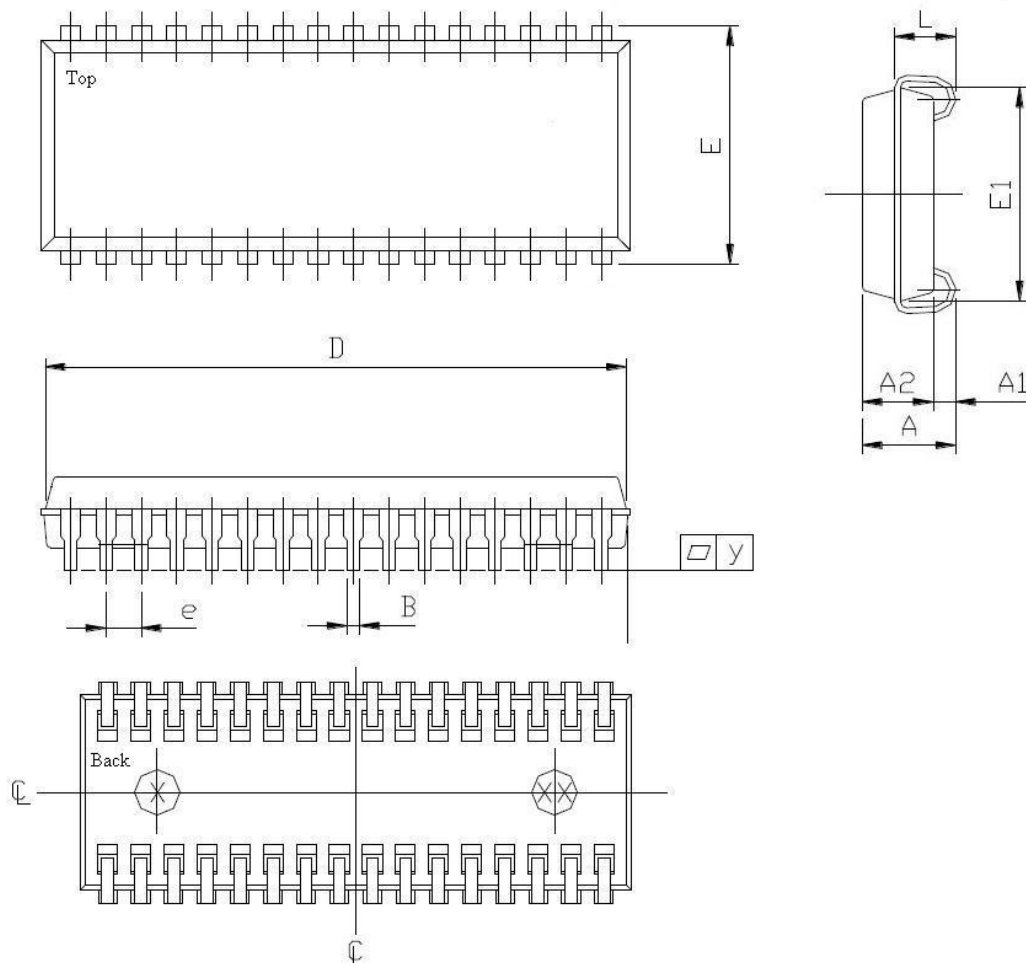


Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

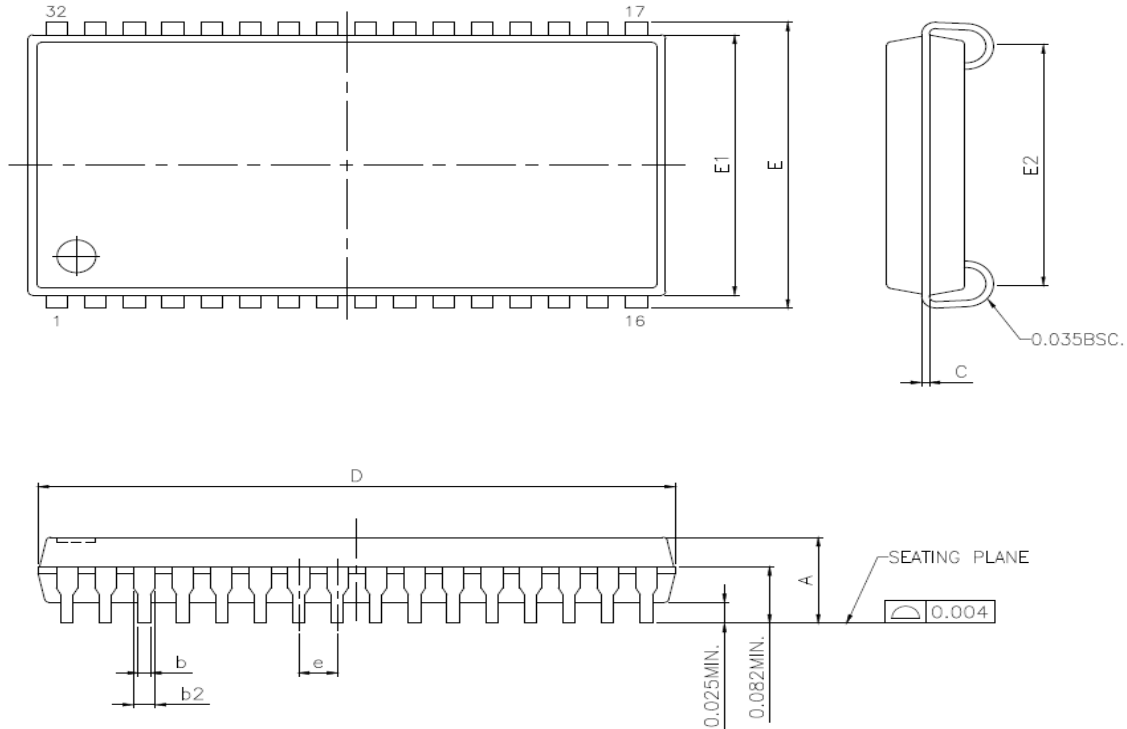
32-pin 300mil SOJ Package Outline Dimension



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.148(MAX)	3.759(MAX)
A1		0.025(MIN)	0.635(MIN)
A2		0.123(MAX)	3.124(MAX)
B		0.018(TYP)	0.457(TYP)
D		0.825±0.005	20.955±0.127
E		0.335(TYP)	8.509(TYP)
E1		0.300±0.005	7.620±0.127
e		0.050(TYP)	1.270(TYP)
L		0.086±0.010	2.184±0.254
y		0.003(MAX)	0.076(MAX)

PACKAGE OUTLINE DIMENSION

32-pin 400mil SOJ Package Outline Dimension



SYMBOL	SPEC		
	Min	Nom	Max.
A	0.128	-	0.148
b	0.015	-	0.02
b2	0.026	-	0.032
c	0.007	-	0.013
e	0.050 Typ		
D	0.820	-	0.83
E	0.435	-	0.445
E1	0.395	-	0.405
E2	0.360	-	0.38

Unit : Inch

Part numbering system

AS7C	1024D	-XX	XX	X	X	XX
SRAM prefix	Device number 1024: 1M (x8) D: revision D	Access time -12 = 12ns	Package: TJ = SOJ 300mils J = SOJ 400mils	Temperature range: I = Industrial, -40° C to 85° C	N=Lead Free and Halogen Free Part	Packing Type None: Tray TR: Reel



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