Revision History

8GB eMMC 153ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release	December. 2025

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1. Overview

1.1 Product Description

Alliance's eMMC combines a feature-wise flash controller and standard NAND flash memory. Its high performance and low power design make the highly-integrated Alliance eMMC a fabulous solution for embedded and portable applications.

The Alliance eMMC leverages industry leading technology and experience in NAND management. In addition, the Alliance eMMC supports the standard eMMC interface as well as the newly introduced eMMC features such as HS400 mode and FFU. By integrating all the advanced techniques, the Alliance -eMMC is able to further enhance the data transferring efficiency and optimize the overall performance for embedded systems.

Available in various densities, the Alliance eMMC offers the features, performance, and flexibility exactly for mobile handset, navigation, automotive infotainment, multi-function printer, and next-generation consumer applications. With extended temperature support and high data reliability, offering easy and rapid design integration, the Alliance eMMC also ideally fits the requirements of point-of-sale terminals, networking and telecommunications equipment, and a variety of leading-edge industrial applications.

1.2 Key Features

- Industrial Standard Interface
  - JEDEC eMMC Standard Version 5.1 Compliant
- eMMC 5.1 Key Features
  - 11-signal interface (including CMD, CLK, DAT[7:0], and RST_n)
  - Programmable bus width: 1-bit, 4-bit, and 8-bit
  - Supports HS400 high speed interface timing mode up to 400MB/s data rate
  - Up to 200MHz clock frequency
  - Supports eMMC Field firmware update (FFU)
  - Supports eMMC production state awareness (PSA)
  - Supports eMMC device health report
  - High-speed, Dual Data Rate Boot support
  - Supports Boot and Alternative Boot Mode
  - Replay Protected Memory Block (RPMB)
  - Trim, Sanitize, Discard, Secure Erase, Secure Trim
  - High Priority Interrupt (HPI)
  - Background Operations
  - Supports Command Queuing
  - Supports Enhanced Strobe in HS400 Mode
  - Supports eMMC Background Operation Control

- Supports eMMC configuration up to 8 general purpose partitions and 4 RPMB regions
- Supports eMMC CMDQ Enhanced Data Task
- Supports eMMC CMDQ Device Management Operation

- Robust Data Protection and Endurance
  - Configurable ECC engine with zero overhead pipeline greatly reduces data loss rates and increases data endurance
  - Enhanced Write Protection with Permanent, Temporary and Power-On protection options
  - StaticDataRefresh and EarlyRetirement technologies ensure the data reliability
  - PowerShield and DataPhoenix technologies support power-down data protection
  - Global wear leveling maximizes product lifespan with minimal wear leveling and write amplification overhead

- Supply Voltage
  - eMMC Interface Power (VCCQ): 1.70 1.95V
  - eMMC Interface Power (VCCQ): 2.7 3.6V [1]
  - NAND Memory Power (CC): 2.7 3.6V

- Dynamic power management technology enables multiple power saving modes

- Densities and Packages
  - Available in 8GB MLC mode density
  - 153-ball standard BGA packages
  - Green Package and RoHS Compliant

- Operating Temperature
  - Industrial Grade: -40°C ~ +85°C

1.3 Product Ordering Information

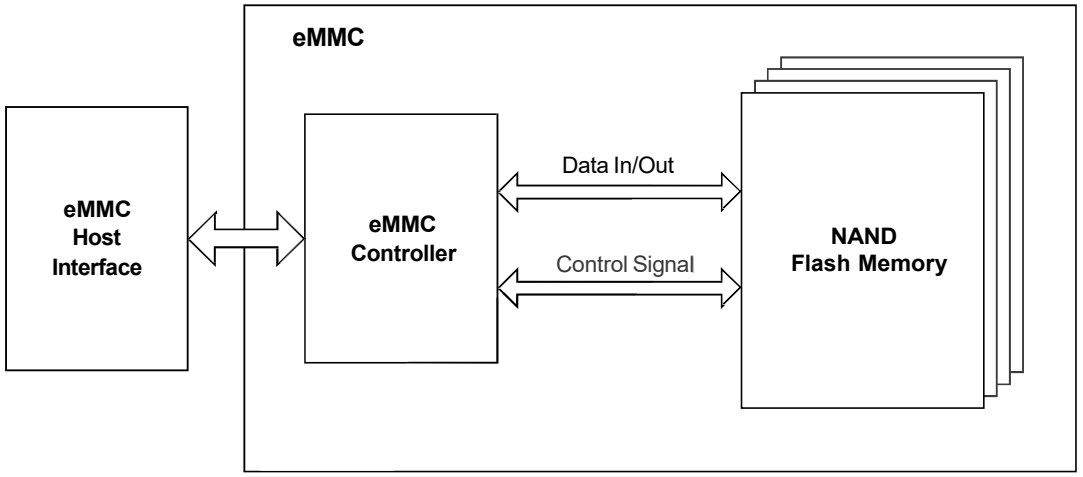
Table 1: Ordering Information

Capacities (GB)	Part Number	eMMC Version	NAND Die	Temperature	Package Size (mm)	Package Type
8	ASFC8G31MB-51BIN	5.1	64Gb x 1	Industrial Grade -40°C ~ +85°C	11.5x13.0x1.199	153ball FBGA

Note1. HS200/HS400 can be supported at only VCCQ 1.8V

1.4 Block Diagram

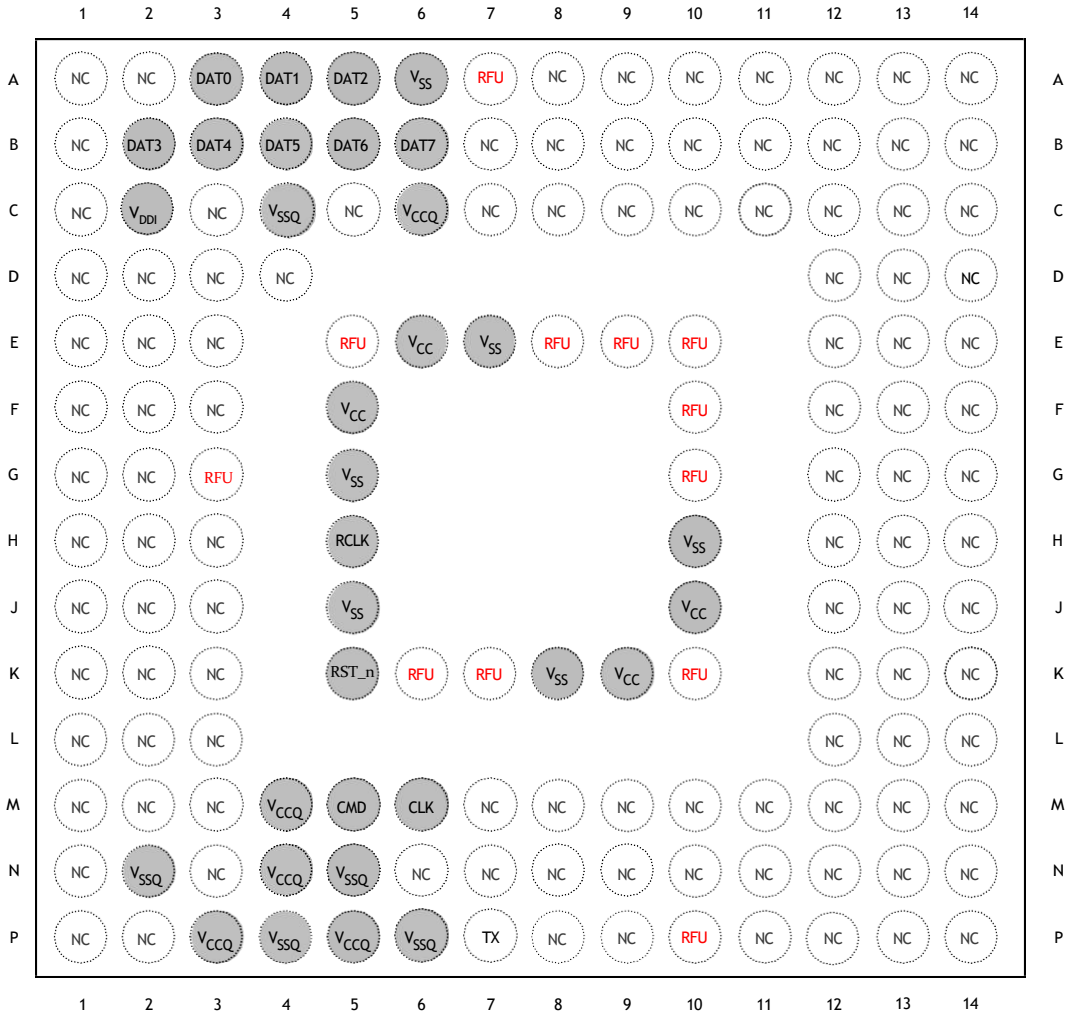
Figure 1: eMMC Block Diagram



2. Pin Assignments and Signal Descriptions

2.1 Pin Assignments

Figure 2: 153-Ball Pin Assignments (Top View - Balls Down)



2.2 Signal Descriptions

Table 2: Functional Signals

Signal	Type	Description
CLK	Input	Clock. Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
RCLK	Output	eMMC interface data strobe (HS400 mode)
CMD	I/O	Command. This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
DAT0 – DAT7	I/O	Data I/O. These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-up or as sertion of the RST_n signal, only DAT0 is used for data transfer. The eMMC controller can configure a wider data bus for data transfer using either DAT[3:0] (4-bit mode) or DAT[7:0] (-bit mode). eMMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Correspondingly, immediately after entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
RST_n	Input	Reset. The RST_n signal is used for host resetting device, moving the device to pre-idle state. By default, the RST_n signal is temporary disabled in device. The host must set bits[1:0] in the extended CSD register [162] to 0x1 to enable this functionality before the host can use it.
VCC	Supply	NAND interface I/O and NAND Flash power supply.
VCCQ	Supply	eMMC controller core and eMMC interface I/O power supply.
VSS	Supply	NAND interface I/O and NAND Flash ground connection.
VSSQ	Supply	eMMC controller core and eMMC interface ground connection.
VDDi	-	Internal voltage node A 1.0uF capacitor is required for VDDi for core power stabilization. Do not tie to supply voltage or ground.
TX	Output	UART Tx output for debug use
NC	-	No connect
RFU	-	Reserved for future use. Leave it floating.

2.3 Pin List

Table 3: Pin List of eMMC Packages

Signal	Pin Number of 153-Ball
CLK	M6
RCLK	H5
CMD	M5
DAT0 – DAT7	A3, A4, A5, B2, B3, B4, B5, B6
RST_n	K5
VCC	E6, F5, J10, K9
VCCQ	C6, M4, N4, P3, P5
VSS	A6, E7, G5, H10, J5, K8
VSSQ	C4, N2, N5, P4, P6
VDDi	C2
TX	P7
NC	A1, A2, A8 - A14, B1, B7 - B14, C1, C3, C5, C7 - C14, D1 - D4, D12 - D14, E1 - E3, E12 - E14, F1 - F3, F12 - F14, G1, G2, G12 - G14, H1 - H3, H12 - H14, J1 - J3, J12 - J14, K1 - K3, K12 - K14, L1 - L3, L12 - L14, M1 - M3, M7 - M14, N1, N3, N6 - N14, P1, P2, P8 - P14
RFU	A7, E5, E8, E9, E10, F10, G3, G10, K6, K7, K10

3. eMMC Registers

This chapter introduces the registers for eMMC and the default register values in the eMMC.

Within the device interface the following registers are defined: OCR, CID, CSD, EXT_CSD, and RCA. These can be accessed only by corresponding commands (see eMMC specification). The OCR, CID and CSD registers carry the device/content specific information, while the RCA register is a configuration register storing actual configuration parameters. The EXT_CSD register carries both, device specific information and actual configuration parameters.

3.1 OCR Register

For eMMC devices, the OCR (operation conditions register) response is fixed as 0x40FF8080 for ASFC8G31MB-51BIN/TR

3.2 CID Register

The CID register is 128 bits wide contains the card identification used during the card idenfication phase.

Table 4: eMMC CID Register

Name	Field	Width	CID-Slice	Value	Note
Manufacturer ID	MID	8	[127:120]	52h	Alliance MiD
Reserved	-	6	[119:114]	00h	
Device/BGA	CBX	2	[113:112]	01h	
OEM/Application ID	OID	8	[111:104]	52h	Alliance MiD
Product name	PNM	48	[103:56]	415330384643h	AS08FC
Product revision	PRV	8	[55:48]	0Ch	RevB
Product serial number	PSN	32	[47:16]	XXh	
Manufacturing date	MDT	8	[15:8]	XXh	
CRC7 checksum	CRC	7	[7:1]	XXh	
Not used, always “1”	-	1	[0:0]	01h	

3.3 Relative Card Address Register (RCA)

The writable 16-bit relative card address register stores the card address. This address is published by the card during card identification, and is used for host-card communication following the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved for setting all cards in the Stand-by State with CMD7.

3.4 CSD Register

The Device-Specific Data (CSD) register defines the behavior of eMMC devices. The eMMC behavior is related to the controller design. The following table shows a typical CSD definition of the eMMC. If users need to add on more features, firmware or hardware modifications may be necessary.

Table 5: eMMC Typical CSD Register

Name	Field	Bit	Type	Slice	Value	Note
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved	-	2	R	[121:120]	-	
Data read access-time-1	TAAC	8	R	[119:112]	27h	
Data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	01h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h	
Device command classes	CCC	12	R	[95:84]	8F5h	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	
DSR implemented	DSR_IMP	1	R	[76:76]	0h	
Reserved	-	2	R	[75:74]	-	
Device size	C_SIZE	12	R	[73:62]	FFFh	
Max. read current at VDD (min)	VDD_R_CURR_MIN	3	R	[61:59]	7h	
Max. read current at VDD (max)	VDD_R_CURR_MAX	3	R	[58:56]	7h	
Max. write current at VDD (min)	VDD_W_CURR_MIN	3	R	[55:53]	7h	
Max. write current at VDD (max)	VDD_W_CURR_MAX	3	R	[52:50]	7h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	

Name	Field	Bit	Type	Slice	Value	Note
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	
Reserved	-	4	-	[20:17]	-	
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag (OTP)	COPY	1	R/W	[14:14]	1h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	
CRC	CRC	7	R/W/E	[7:1]	-	
Not used, always '1'	-	1	-	[0:0]	1h	

Notes:

1. The definitions of cell type are shown as follows:
   R: Read only.
   W: One time programmable and not readable.
   R/W: One time programmable and readable.
   W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
   R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
   R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
   W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.
2. Reserved bits should be read as “0”.
3. The column marked with “-“ is undefined.

3.5 Extended CSD Register (EXT_CSD)

The Extended CSD register defines the additional behavior of eMMC devices due to limited CSD information. The following table shows a typical extended CSD definition of the Alliance-eMMC. If users need to add on more features, firmware or hardware modifications may be necessary. The register is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in.

Table 6: eMMC Typical EXT_CSD Register

Name	Field	Byte	Type	Slice	Value	Note
Reserved	-	6	-	[511:506]	-	
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0h	
Supported command sets		1	R	[504]	1h	Allocated by MMCA
HPI features	HPI_FEATURES	1	R	[503]	1h	HPI type CMD13
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h	BKOPS supported
Max packed read commands	MAX_PACKED_READS	1	R	[501]	20h	
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	20h	
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h	
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0h	
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0h	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	78h	
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	1h	
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	3h	
Supported modes	SUPPORTED_MODES	1	R	[493]	1h	
FFU features	FFU_FEATURES	1	R	[492]	0h	
Operation codes timeout	OPERATION_CODE_TIME OUT	1	R	[491]	17h	
FFU Argument	FFU_ARG	4	R	[490:487]	FFFAFFF0h	
Barrier support	BARRIER_SUPPORT	1	R	[486]	1h	
Reserved	-	177	-	[485:309]	-	
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	1h	
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	1Fh	
Reserved	-	1	-	[306]	-	
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTOR S_CORRECTLY_PROGRAM MED	4	R	[305:302]	0000h	
Vendor proprietary health report	VENDOR_PROPRIETARY_ HEALTH_REPORT	32	R	[301:270]	-	

Name	Field	Byte	Type	Slice	Value	Note
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	01h	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	01h	
Pre EOL information	PRE_EOL_INFO	1	R	[267]	01h	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	40h	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	40h	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	07h	
Device version	DEVICE_VERSION	2	R	[263:262]	See Note	8GB: 0805h
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	See Note	00 00 00 00 00 00 00 01
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h	
Cache size	CACHE_SIZE	4	R	[252:249]	0400h	
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	5h	
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	64h	
Background operations status	BKOPS_STATUS	1	R	[246]	0h	No operations required
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h	
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0Ah	Initial time out 1s
Cache Flushing Policy	CACHE_FIUSH_POLICY	1	R	[240]	1h	
Power class for 52MHz, DDR at VCC=3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h	RMS 100mA, Peak 200mA
Power class for 52MHz, DDR at VCC=1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h	RMS 65mA, Peak 130mA
Power class for 200MHz at VCCQ=1.95V, VCC=3.6V	PWR_CL_200_195	1	R	[237]	0h	
Power class for 200MHz, at VCCQ=1.3V, VCC=3.6V	PWR_CL_200_130	1	R	[236]	0h	
Minimum write performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h	For cards not reaching the 4.8MB/s value
Minimum read performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h	For cards not reaching the 4.8MB/s value
Reserved	-	1	-	[233]	-	
TRIM multiplier	TRIM_MULT	1	R	[232]	02h	Trim time out 600ms

Name	Field	Byte	Type	Slice	Value	Note
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h	1. Support the secure and insecure trim operations. 2. Support the automatic secure purge operation on retired defective portions of the array. 3. Secure purge operations are supported.
Secure Erase multiplier	SEC_ERASE_MULT	1	R	[230]	19h	
Secure TRIM multiplier	SEC_TRIM_MULT	1	R	[229]	Ah	
Boot information	BOOT_INFO	1	R	[228]	7h	
Reserved	-	1	-	[227]	-	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	See Note	8GB: 20h
Access size	ACC_SIZE	1	R	[225]	6h	
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	1h	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	2h	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	01h	
High-capacity write group size	HC_WP_GRP_SIZE	1	R	[221]	10h	
Sleep current (VCC)	S_C_VCC	1	R	[220]	7h	
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	7h	
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	17h	
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	12h	
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0Ch	
Sector count	SEC_COUNT	4	R	[215:212]	See Note	8GB: E94000h
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	1h	
Minimum write performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0h	
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0h	
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h	

Name	Field	Byte	Type	Slice	Value	Note
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h	
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0h	
Minimum read performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0h	
Reserved	-	1	-	[204]	-	
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0h	
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0h	
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0h	
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0h	
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	4h	
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	Ah	
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	1Fh	
Device type	DEVICE_TYPE	1	R	[196]	57h	
Reserved	-	1	-	[195]	-	
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	2h	
Reserved	-	1	-	[193]	-	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	8h	
Command set	CMD_SET	1	R/W/E_P	[191]	0h	
Reserved	-	1	-	[190]	-	
Command set revision	CMD_SET_REV	1	R	[189]	0h	
Reserved	-	1	-	[188]	-	
Power class	POWER_CLASS	1	R/W/E_P	[187]	5h	
Reserved	-	1	-	[186]	-	
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0h	
Strobe Support	STROBE_SUPPORT	1	R	[184]	1h	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0h	
Reserved	-	1	-	[182]	-	
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0h	
Reserved	-	1	-	[180]	-	
Partition configuration	PARTITION_CONFIG	1	R/W/E R/W/E_P	[179]	0h	
Boot config protection	BOOT_CONFIG_PROT	1	R/W R/W/C_P	[178]	0h	

Name	Field	Byte	Type	Slice	Value	Note
Boot bus conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0h	
Reserved	-	1	-	[176]	-	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0h	
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0h	
Boot area write protection register	BOOT_WP	1	R/W R/W/C_P	[173]	0h	
Reserved	-	1	-	[172]	-	
User area write protection register	USER_WP	1	R/W R/W/C_P R/W/E_P	[171]	0h	
Reserved	-	1	-	[170]	-	
FW configuration	FW_CONFIG	1	R/W	[169]	0h	
RPMB size	RPMB_SIZE_MULT	1	R	[168]	See Note	8GB: 20h
Write reliability setting register	WR_REL_SET	1	R/W	[167]	1Fh	
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	15h	
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0h	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h	
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0h	
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0h	
HPI_management	HPI_MGMT	1	R/W/E_P	[161]	0h	
Partitioning support	PARTITIONING_SUPPORT	1	R	[160]	7h	
Max enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	See Note	Not support
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h	
Partitioning setting	PARTITION_SETTING_ COMPLETED	1	R/W	[155]	0h	
General purpose partition size	GP_SIZE_MULT	12	R/W	[154:143]	0h	
Reserved	-	3	R/W	[142:140]	0h	
Reserved	-	4	R/W	[139:136]	0h	
Reserved	-	1	-	[135]	-	
Bad block management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h	
Production state awareness	PRODUCTION_STATE_AW ARENESS	1	R/W/E	[133]	0h	
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0h	

Name	Field	Byte	Type	Slice	Value	Note
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0h	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0h	
Reserved	-	2	-	[129:128]	-	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	C8h	
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	1h	
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0h	
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0Ah	
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0h	
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0h	
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	00h	
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	00h	
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	00h	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0h	
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0h	
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0h	
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h	
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0h	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0h	
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0h	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0h	
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h	
Reserved	-	2	-	[28:27]	-	
FFU status	FFU_STATUS	1	R	[26]	0h	
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0h	
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	See Note	8GB: E94000h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	01h	
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	3Bh	

Name	Field	Byte	Type	Slice	Value	Note
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h	
Reserved	-	15	-	[14:0]	-	

Notes:

1. The definitions of cell type are shown as follows:
   R: Read only.
   W: One time programmable and not readable.
   R/W: One time programmable and readable.
   W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
   R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
   R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
   R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
   W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.
2. Reserved bits should be read as “0”.
3. The column marked with “-“ is undefined.

4. DC Electrical Characteristics

Table 7: Operating Conditions

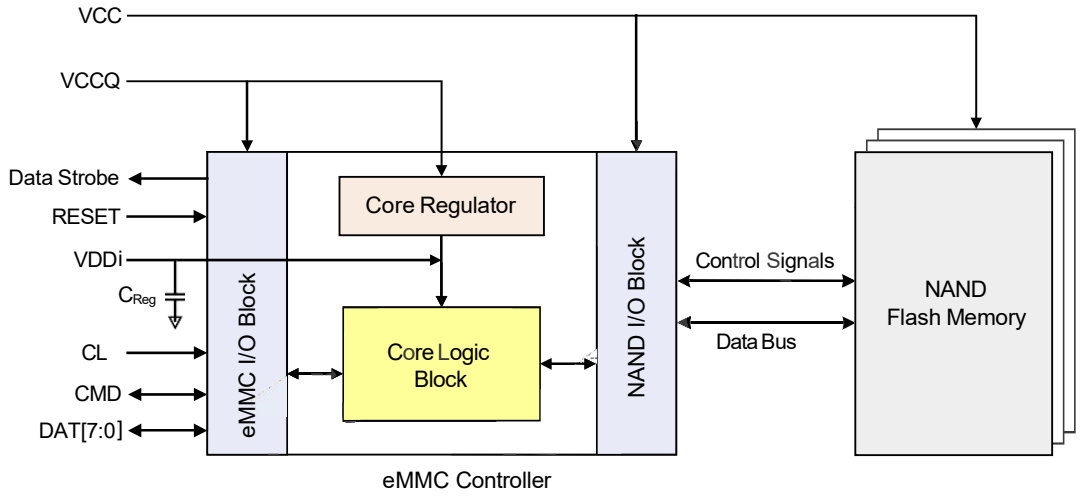
Parameter	Symbol	Min	Max	Unit
Supply Voltage (NAND)	VCC	2.7	3.6	V
Supply Voltage (I/O)	VCCQ	1.7	1.95	V
		2.7	3.6	V
Supply Power-up for 3.3V	tPRUH		35	ms
Supply Power-up for 1.8V	tPRUL		25	ms
Operating Temperature (Industrial Grade)	T_{OPR}	-40	+85	°C

Table 8: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Voltage Input	V_{IN}	-0.3	4.0	V
VCC Supply	VCC	-0.3	4.0	V
VCCQ Supply	VCCQ	-0.3	4.0	V
Storage Temperature (Industrial Grade)	T_{STG}	-40	+85	°C

In the Alliance-eMMC, VCC is used for the NAND flash device; and VCCQ is for the controller and the eMMC interface voltage. A C_{Reg} capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

Figure 3: Internal Power Diagram (Example)



5. Product Specifications

5.1 Capacity

The following table shows the capacity related specifications.

Table 9: User Capacity

NAND Type	Capacity	Sector Count (Hex)	Byte (Decimal)	Capacity Utilization Rate
MLC	8GB	0xE94000	7,826,571,264	91%

The following table shows the size of boot partitions and RPMB.

Table 10: Boot Partition and RPMB

Capacity	Boot Partition 1	Boot Partition 2	RPMB	Note
8GB	4,096KB	4,096KB	4,096KB	14nm MLC with LDPC

5.2 Power Consumption

The power consumption of eMMC is measured in HS400 mode.

Table 11: Power Consumption for Read and Write

Capacity	VCC Current		VCCQ Current		Unit
	Read	Write	Read	Write	
8GB	85	60	170	80	mA

Table 12: Power Consumption for Sleep and APS Modes

Capacity	VCC Current		VCCQ Current		Unit
	Sleep	APS	Sleep	APS	
8GB	30	45	80	80	μA

Notes:

1. VCC/VCCQ current listed in Table 12 and/or Table 13 is the typical value.
2. Conditions:
   - 8-bit bus width in HS400 mode
   - VCCQ 1.8V
   - Room temperature
3. The measurement of current is presented as RMS (Root Mean Square) value.
4. APS: Auto Power-Saving mode. When Alliance-eMMC finds that the host has not sent a command in 20ms, it will enter APS mode to save power.

5.3 Performance

Table 13: MLC Mode Performance at HS400

NAND Flash	Capacity	Random Read	Random Write	Sequential Read	Sequential Write
14nm MLC	8GB (64Gb/1 Die)	14000 IOPS	17000 IOPS	280 MB/s	110 MB/s

Table 14: MLC Mode Performance at HS200

NAND Flash	Capacity	Random Read	Random Write	Sequential Read	Sequential Write
14nm MLC	8GB (64Gb/1 Die)	12000 IOPS	17000 IOPS	170 MB/s	110 MB/s

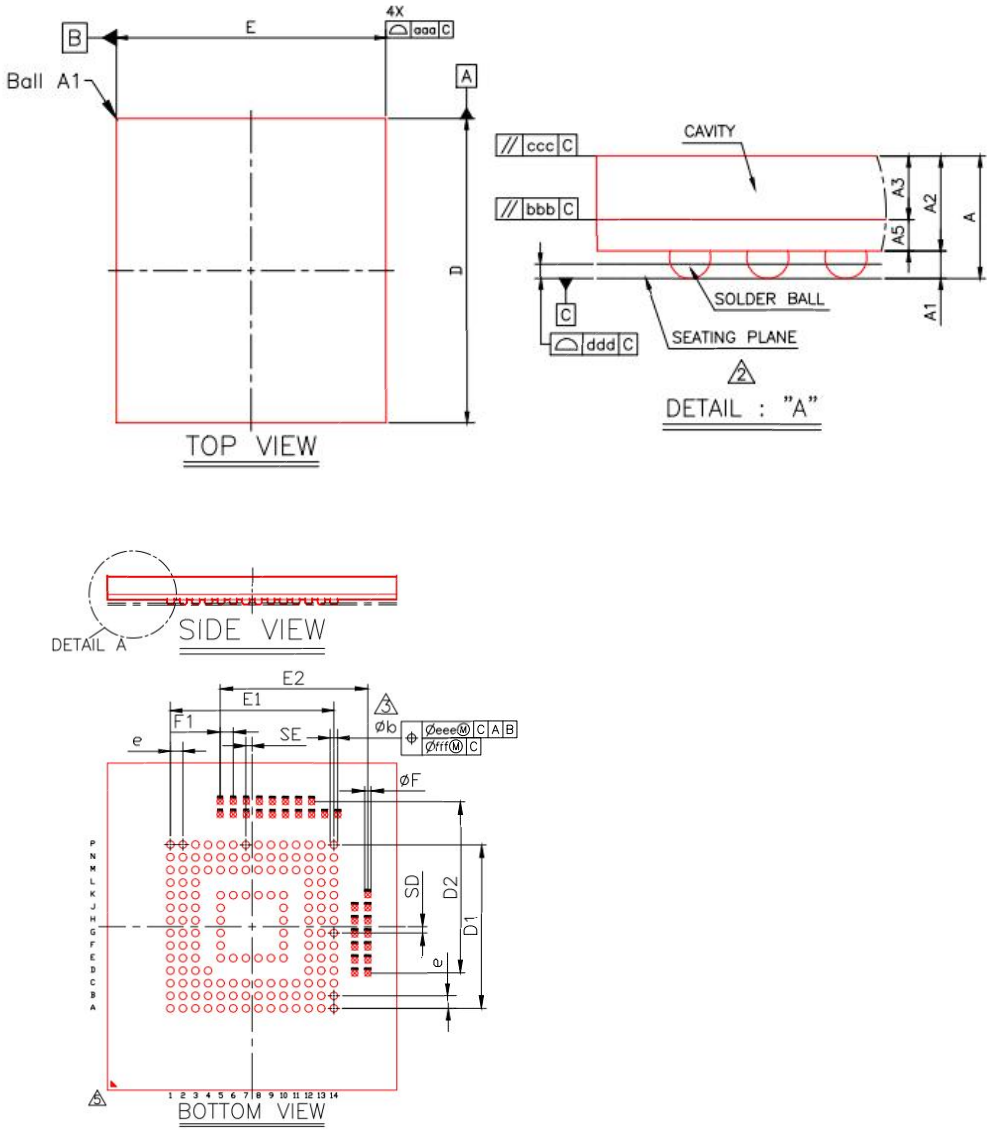
5.4 Endurance

Table 15: Program/Erase Cycle Count

NAND Flash	P/E Cycle in MLC Mode
14nm MLC	3K

6. Package Outline Information

Figure 4: 153-Ball BGA Package Outline (11.5mm x 13mm x 1.199mm)



Symbol	MIN	NOM	MAX	Symbol	MIN	NOM	MAX
A	1.061	1.130	1.199	b	0.250	0.300	0.350
A1	0.160	0.210	0.260	F	---	0.250	---
A2	0.873	0.920	0.967	F1	---	0.520	---
A3	0.685	0.710	0.735	aaa		0.150	
A5	0.170	0.210	0.250	bbb		0.100	
E	11.400	11.500	11.600	ccc		0.150	
D	12.900	13.000	13.100	ddd		0.080	
E1	---	6.500	---	eee		0.150	
D1	---	6.500	---	fff		0.050	
E2	---	5.870	---	MD/ME		14/14	
D2	---	6.820	---	SE		0.250	
e	---	0.500	---	SD		0.250	

Notes:
1. Controlling dimension: Millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: ccc, ddd.
5. The pattern of Pin 1 fiducial is for reference only.
6. Ball placement use 0.300 mm solder ball. BGA pad solder mask opening = 0.275 mm.
7. This PKG is 153 balls + 31 test pins.

7. Part number system

Table 16: Part number system

AS	FC	8G	3	1	M	B	-51	B	I	N	XX
Alliance Memory	eMMC Series (Flash + Controller)	Density 4G=4GB 8G=8GB 16G=16GB	Flash Voltage 3=3.3V 1=1.8V	NAND Die 1=Single 2=Dual Die	NAND Type S = SLC M = MLC	Generation Code Blank = rev0 A = revA B = revB	eMMC Version 51 = 5.1	Package Type B = 153b FBGA (11.5x13mm)	Operating Temperature I = Industrial (-40°C~85°C)	ROHS Compliant	Packing Type None:Tray TR:Reel

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