Revision History

4Gb(x32) LPDDR4x 200ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release	Sept. 2025

Overview

The LPDDR4X SDRAM is organized as 1 or 2 channels per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

This LPDDR4X device uses a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock.

Features

- JEDEC standard Compliant
- Fast clock rate: 1200/1600 MHz
- Low-voltage Core and I/O Power Supplies:
  - V_{DD1} = 1.8V (1.7V~1.95V)
  - V_{DD2} = 1.1V (1.06V~1.17V)
  - V_{DDQ} = 0.6V (0.57V~0.65V)
- Operating Temperature:
  - T_C = -40 ~ 85°C (Industrial)
- Supports JEDEC clock jitter specification
- On-Chip ECC:
  - Single-bit error correction (per 64-bits), which will maximize reliability
  - Optional ERR output signal per channel, which indicates ECC event occurrence
  - ECC Register, which controls ECC function
- Configuration:
  - x32 for 2-channels per device

  8 internal banks per each channel
- 16n-bit prefetch architecture
- Single data rate (multiple cycles) CMD/ADR bus
- Bidirectional/differential data strobe per byte of data DQS/DQS#
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies
- Programmable and on-the-fly burst lengths
- Support non-targert DRAM ODT control
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Selectable output drive strength (DS)
- Dynamic ODT :
  - DQ ODT: VSSQ Termination
  - CA ODT: VSS Termination
- On-chip temperature sensor to control self refresh rate
- On-chip temperature sensor whose status can be read from MR4
- Interface: LVSTL
- Internal VREF and VREF Training
- ZQ Calibration
- RoHS compliant
- 200-ball x32 Discrete Package 10x14.5x0.8mm (max)
  - Pb and Halogen Free

Table 1. Ordering Information

Part No.	Density	Org.	Package	Temperature	Max Frequency
AS4C128M32MD4VA-062BIN	4Gb	2ch x16	10x14.5x0.8mm(Max), 200-FBGA	Tc = -40 ~ 85°C	1600 MHz

Package Block Diagram

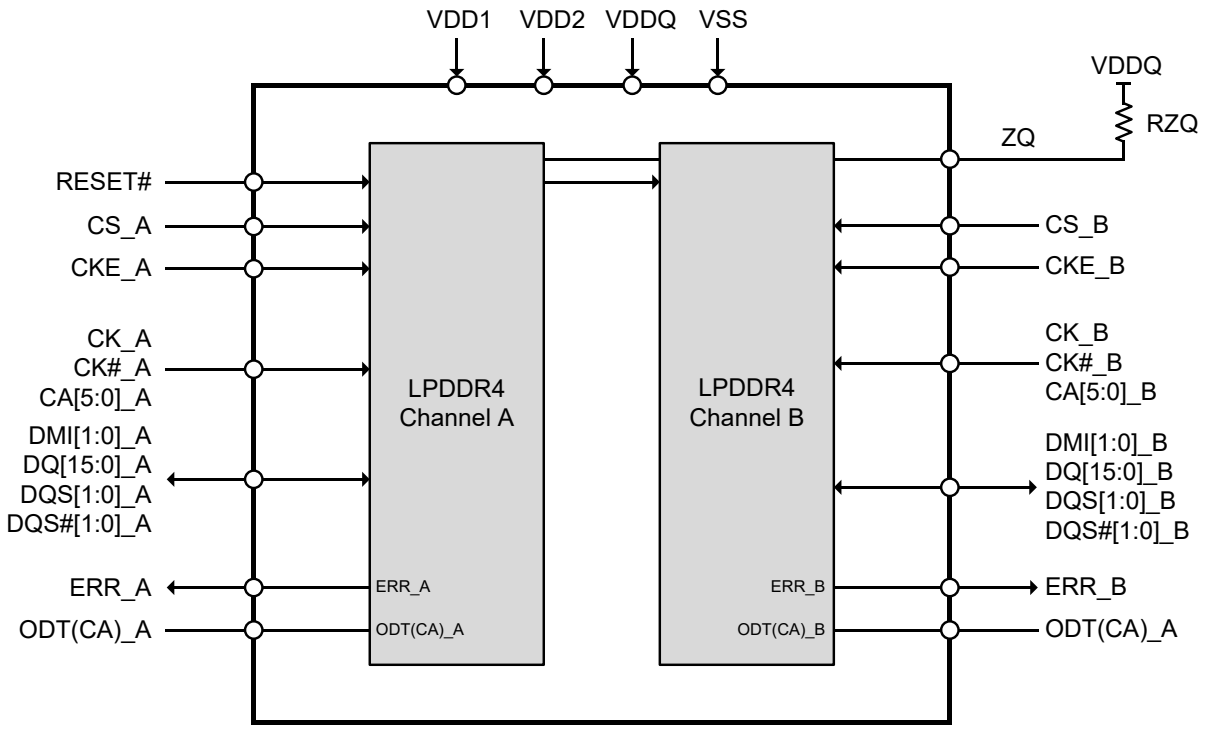
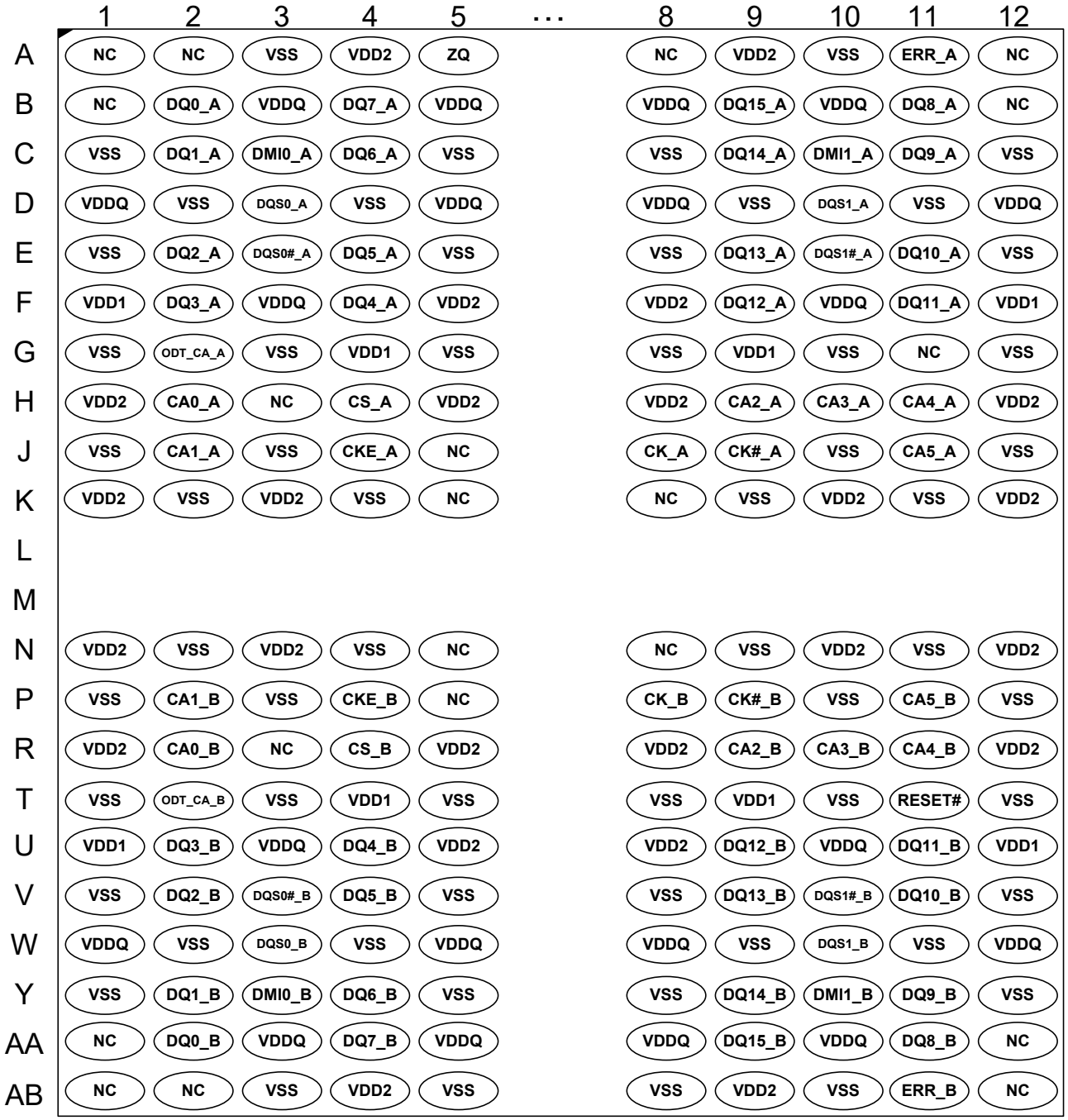


Figure 1. Dual Channel Package Block Diagram (x32)

Ball Assignment



	1	2	3	4	5	…	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ		NC	VDD2	VSS	ERR_A	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ		VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS		VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_A	VSS	VDDQ		VDDQ	VSS	DQS1_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0#_A	DQ5_A	VSS		VSS	DQ13_A	DQS1#_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2		VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS		VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	NC	CS_A	VDD2		VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE_A	NC		CK_A	CK#_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC		NC	VSS	VDD2	VSS	VDD2
L											
M											
N	VDD2	VSS	VDD2	VSS	NC		NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE_B	NC		CK_B	CK#_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	NC	CS_B	VDD2		VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS		VSS	VDD1	VSS	RESET#	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2		VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0#_B	DQ5_B	VSS		VSS	DQ13_B	DQS1#_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_B	VSS	VDDQ		VDDQ	VSS	DQS1_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS		VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	NC	DQ0_B	VDDQ	DQ7_B	VDDQ		VDDQ	DQ15_B	VDDQ	DQ8_B	NC
AB	NC	NC	VSS	VDD2	VSS		VSS	VDD2	VSS	ERR_B	NC

NOTE 1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
NOTE 2 Top View, A1 in top left corner.
NOTE 3 ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
NOTE 4 Die pad VSS and VSSQ signals are combined to VSS package balls.
NOTE 5 11A and 11AB are optional ERR signals.

Figure 2. 200-Ball x32 (FBGA Top View)

Addressing

Table 2. LPDDR4X SDRAM Addressing

Memory Density		128Mx32 (4Gb/Package)
Organization		x32
Number of Channels		2
Density per channel		2Gb
Configuration		16Mb x 16DQ x 8 banks x 2 channels
Number of Banks (per Channel)		8
Array Pre-Fetch (Bits, per channel)		256
Number of Rows (per channel)		16,384
Number of Columns (fetch boundaries)		64
Page Size (Bytes)		2048
Bank Address		BA0-BA2
x16	Row Addresses	R0-R13
	Column Addresses	C0-C9
Burst Starting Address Boundary		64-bit

Note 1. The lower two column addresses (C0 - C1) are assumed to be “zero” and are not transmitted on the CA bus.
Note 2. Row and Column address values on the CA bus that are not used for a particular density be at valid logic levels.
Note 3. For non - binary memory densities,only half of the row address space is valid. When the MSB address bit is “HIGH”, then the MSB - 1 address bit must be “LOW”.

Ball Descriptions

Table 3. Ball Details

Symbol	Type	Description
CK_A, CK#_A, CK_B, CK#_B	Input	**Clock:** CK and CK# are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A, CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A, CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. ODT-CS/CA/CK function is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS.
DQ[15:0]_A, DQ[15:0]_B	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0]_A, DQS#1:0]_A, DQS[1:0]_B, DQS#1:0]_B	I/O	**Data Strobe:** DQS and DQS# are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDD1, VDD2, VDDQ	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference.
RESET#	-	**RESET:** When asserted LOW, the RESET# signal resets all channels of the die. There is one RESET# pad per die.
NC	-	**No connect**: Not internally connected.

Note 1. "_A" and "_B" indicate DRAM channel "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only.

Truth Tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.
CKE signal has to be held high when the commands listed in the command truth table input.

Table 4. Command Truth Table

	Command Pins	CA Pins							
Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK Edge	Notes
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1~4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1~4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	L	R1	1,2
	L	V						R2	
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1~3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1~3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	L	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1~3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write -2, Read- 2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write - 1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write- 2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read- 1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	X	R1	1~3,10
	L	BA0	BA1	BA2	X	R10	R11	R2	
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

Note 1. All LPDDR4X commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
Note 2. "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
Note 3. Bank addresses BA[2:0] determine which bank is to be operated upon.
Note 4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
Note 5. Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
Note 6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an Auto-Precharge will occur to the bank associated with the Write, Mask Write or Read command.
Note 7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".

Note 8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.

Note 9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.

Note 10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.

Note 11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.

Note 12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

Power-up, Initialization, and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as the table below.

Table 5. MRS defaults settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0_B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000_B	WL = 4
RL	MR2 OP[2:0]	000_B	RL = 6, nRTP=8
nWR	MR1 OP[6:4]	000_B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00_B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000_B	DQ ODT is disabled
VREF(CA) Setting	MR12 OP[6]	1_B	VREF(CA) Range[1] enabled
VREF(CA) Value	MR12 OP[5:0]	001101_B	Range1 : 50.3% of VDD2
VREF(DQ) Setting	MR14 OP[6]	1_B	VREF(DQ) Range[1] enabled
VREF(DQ) Value	MR14 OP[5:0]	001101_B	Range1 : 50.3% of VDDQ

Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4X device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET# is recommended to be LOW (≤ 0.2 x VDD2) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET# is held LOW. Power supply voltage ramp requirements are provided in the table below. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

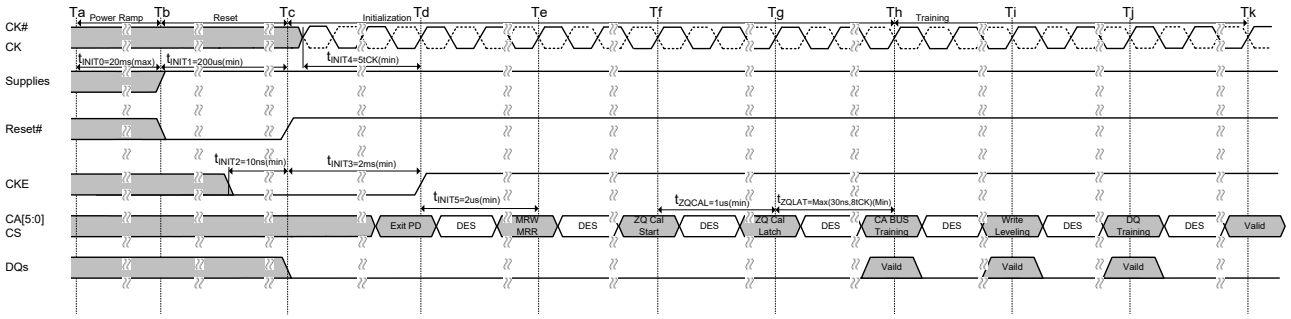
Table 6. Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ - 200 mV

Note 13. Ta is the point when any power supply first reaches 300 mV.
Note 14. Voltage ramp conditions in Table 8 apply between Ta and power-off (controlled or uncontrolled).
Note 15. Tb is the point at which all supply and reference voltages are within their defined ranges.
Note 16. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
Note 17. Thevoltage difference between any of VSS and VSSQ pins must not excess 100 mV.

2. Following the completion of the voltage ramp (Tb), RESET# must be maintained LOW. DQ, DMI, DQS and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latch-up. CKE, CK, CK#, CS and CA input levels must be between VSS and VDD2 during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET# must remain LOW for at least tINIT1 (Tc), after which RESET# can be deasserted to HIGH (Tc). At least 10ns before RESET# de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".



Note 1. Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

Figure 3. Power Ramp and Initialization Sequence

4. After RESET# is de-asserted (Tc), wait at least tINIT3 before activating CKE. Clock (CK, CK#) is required to be started and stabilized for tINIT4 before CKE goes active (Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4X DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4X device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4X device will power-up with receivers configured for low-speed operations, and VREF (CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS timing to the point where the device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(DQ)(Tj). The device will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table 7. Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage ramp time
t_{INIT1}	200	-	us	Minimum RESET# LOW time after completion of voltage ramp
t_{INIT2}	10	-	ns	Minimum CKE low time before RESET# high
t_{INIT3}	2	-	ms	Minimum CKE low time after RESET# high
t_{INIT4}	5	-	t_{CK}	Minimum stable clock before first CKE high
t_{INIT5}	2	-	us	Minimum idle time before first MRW/MRR command
t_{ZQCAL}	1	-	us	ZQ calibration time
t_{ZQLAT}	Max(30ns, $8t_{CK}$)	-	ns	ZQCAL latch quiet time
t_{CKb}	Note *1,2	Note *1,2	ns	Clock cycle time during boot

Note:
1. Min tCKb guaranteed by DRAM test is 18 ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.
1. Assert RESET# below 0.2 x VDD2 anytime when reset is needed. RESET# needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET#.
2. Repeat steps 4 to 10 in Voltage Ramp section.

Table 8. Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
t_{PW_RESET}	100	-	ns	Minimum RESET# low Time for Reset Initialization with stable power

Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (0.2 × V_{DD2}) and all other inputs must be between V_{ILmin} and V_{IHmax}. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS, and DQS# voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. RESET#, CK, CK#, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 9. Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV

The voltage difference between V_{SS}, $V_{SSQ,}$ and V_{SSCA} must not exceed 100mV.

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 10. Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	t_{POFF}	-	2	s

Read and Write Access Operations

After a bank has been activated, a read or write command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) at a rising edge of CK.

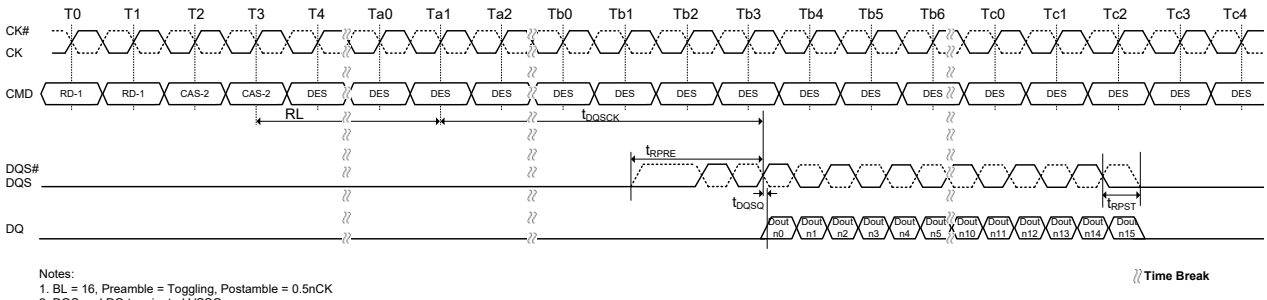
The LPDDR4X-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly (see Command Truth Table).

Read Preamble and Postamble

The DQS strobe for the LPDDR4X requires a pre-amble prior to the first latching edge (the rising edge of DQS with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

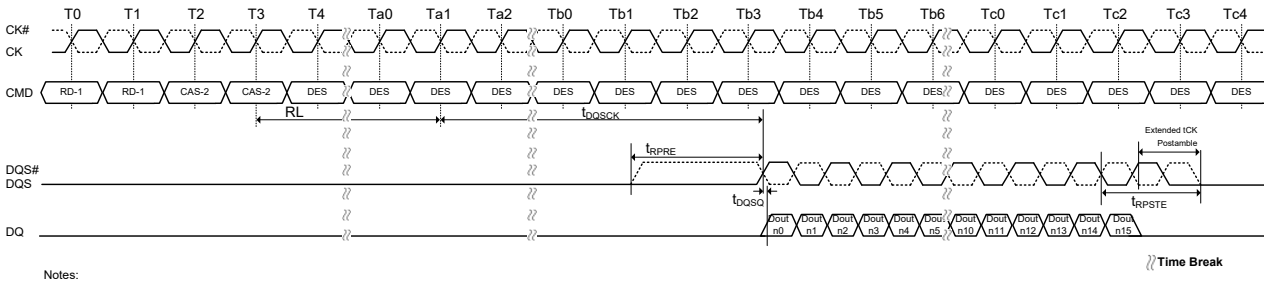
For Read operations the pre-amble is 2*tCK, but the pre-amble is static (no-toggle) or toggling, selectable via mode register.

LPDDR4X will have a DQS Read post-amble of 0.5*tCK (or extended to 1.5*tCK). Standard DQS postamble will be 0.5*tCK driven by the DRAM for Reads. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Read post-amble. The drawings below show examples of DQS Read post-amble for both standard (tRPST) and extended (tRPSTE) post-amble operation.



Notes:
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS and DQ terminated VSSQ.
3. DQS#/DQS is "don't care" prior to the start of tRPRE.
No transition of DQS is implied, as DQS#/DQS can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure 4. DQS Read Preamble and Postamble: Toggling Preamble and 0.5nCK Postamble



Notes:
1. BL = 16, Preamble = Static, Postamble = 1.5nCK (Extended)
2. DQS and DQ terminated VSSQ.
3. DQS#/DQS is "don't care" prior to the start of tRPRE.
No transition of DQS is implied, as DQS#/DQS can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure 5. DQS Read Preamble and Postamble: Static Preamble and 1.5nCK Postamble

Burst Read Operation

A burst Read command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be “0”, so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC). The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL * tCK + tDQSCK + tDQSQ after the rising edge of Clock that completes a read command. The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e., post-preamble) rising edge of the data strobe. Each subsequent data out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle postamble if the programmable post-amble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS and DQS#.

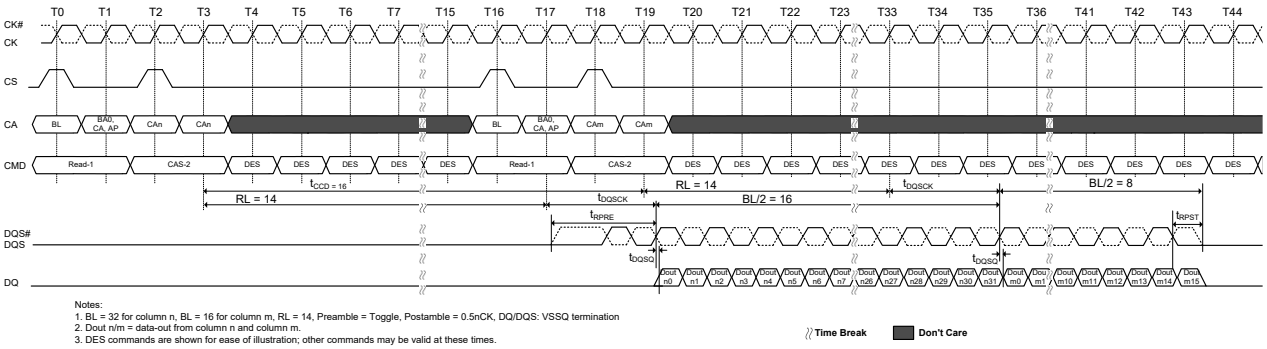


Figure 6. Burst Read Timing

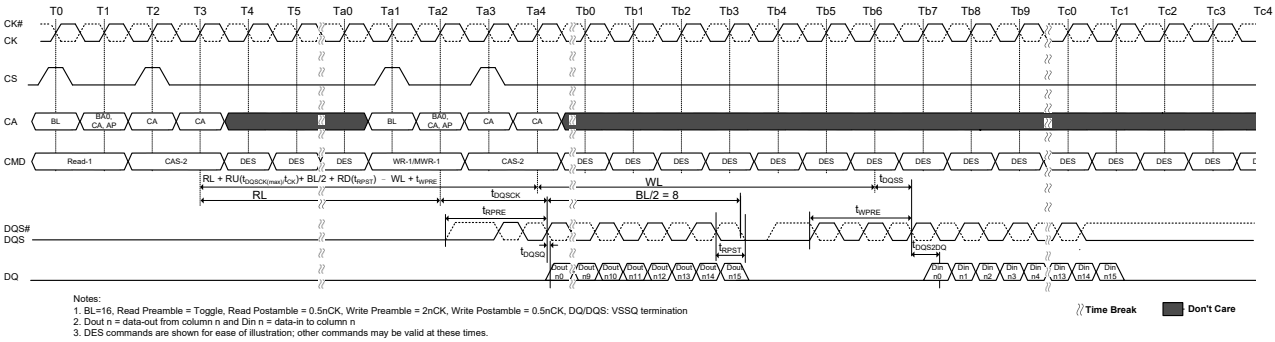
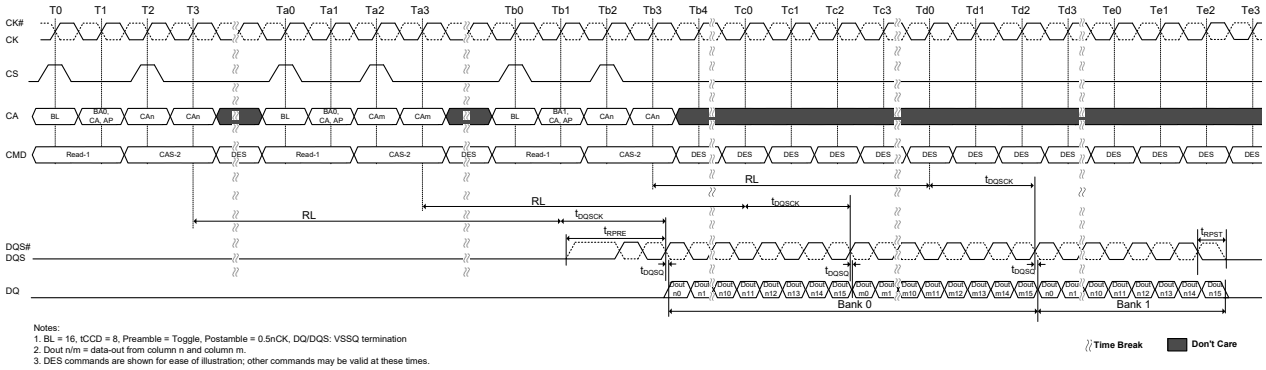


Figure 7. Burst Read followed by Burst Write or Burst Mask Write

The minimum time from a Burst Read command to a Write or MASK WRITE command is defined by the read latency (RL) and the burst length (BL).
Minimum Read-to-Write or Mask Write latency is RL+RU(tDQSCK(max)/tCK)+BL/2+RD(tRPST)-WL+tWPRE.

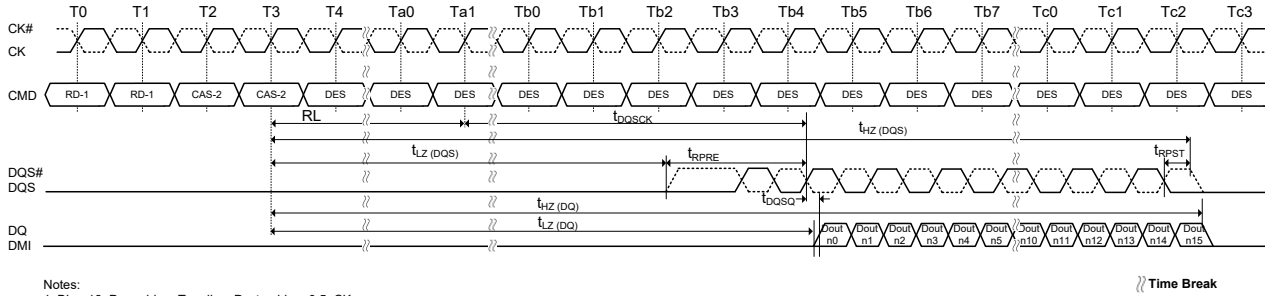


Notes:
1. BL = 16, tCCD = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 8. Seamless Burst Read

The seamless Burst Read operation is supported by placing a Read command at every tCCD(Min) interval for BL16 (or every 2 x tCCD(Min) for BL32).

The seamless Burst Read can access any open bank.



Notes:
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS, DQ and DMI terminated VSSQ.
3. Output driver does not turn on before an end point of tLZ(DQS) and tLZ(DQ).
4. Output driver does not turn off before an end point of tHZ(DQS) and tHZ(DQ)

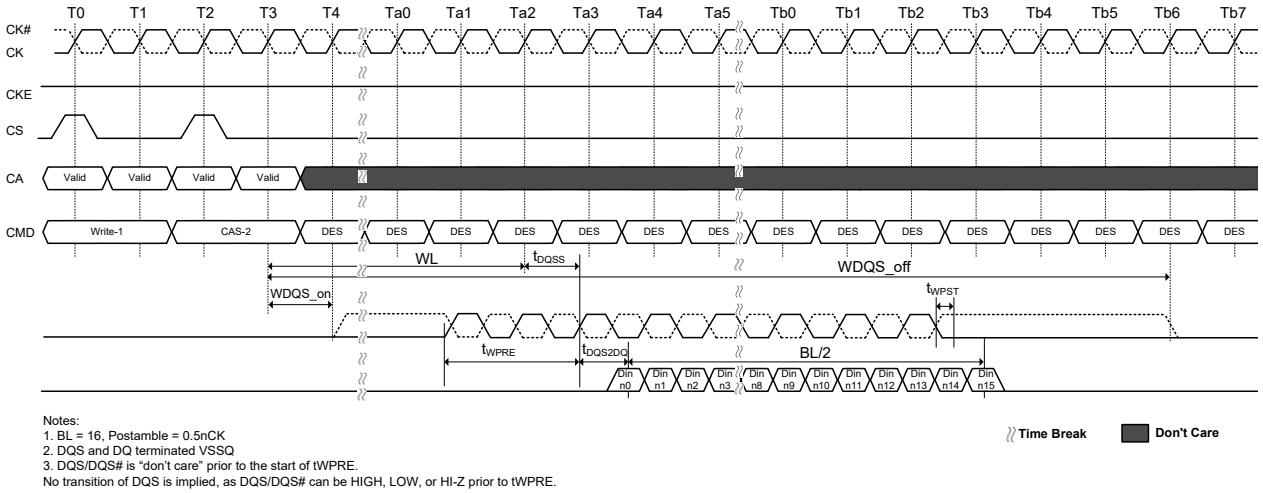
Figure 9. Read Timing

Write Preamble and Postamble

The DQS strobe for the LPDDR4X requires a pre-amble prior to the first latching edge (the rising edge of DQS with DATA "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

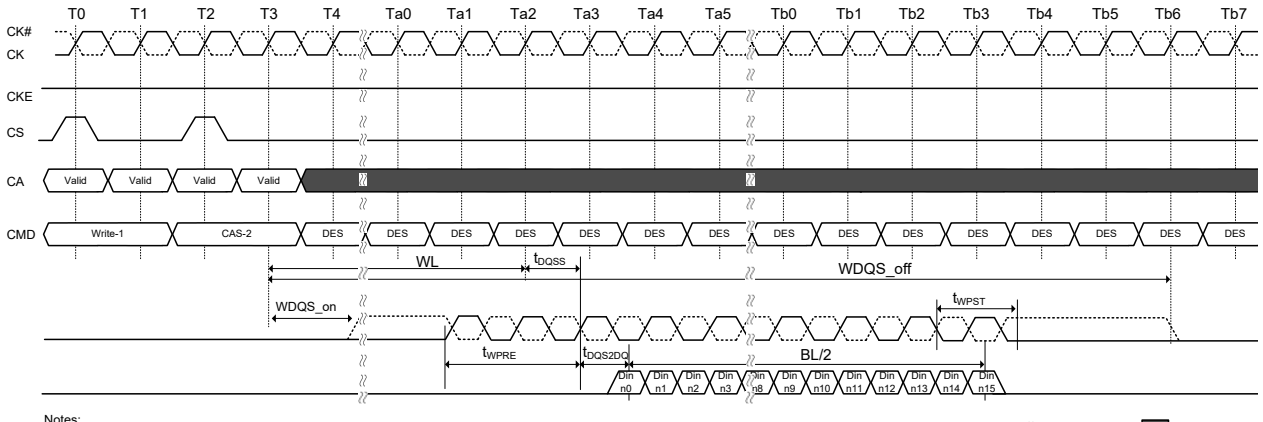
For Write operations, a 2*tCK pre-amble is required at all operating frequencies.

LPDDR4X will have a DQS Write post-amble of 0.5*tCK or extended to 1.5*tCK. Standard DQS post-amble will be 0.5*tCK driven by the memory controller for Writes. A mode register setting instructs the DRAM to drive an additional (extended) one cycle DQS Write post-amble. The drawings below show examples of DQS Write post-amble for both standard (tWPST) and extended (tWPSTE) post-amble operation.



Notes:
1. BL = 16, Postamble = 0.5nCK
2. DQS and DQ terminated VSSQ
3. DQS/DQS# is “don’t care” prior to the start of tWPRE.
No transition of DQS is implied, as DQS/DQS# can be HIGH, LOW, or HI-Z prior to tWPRE.

Figure 10. DQS Write Preamble and Postamble: 0.5nCK Postamble



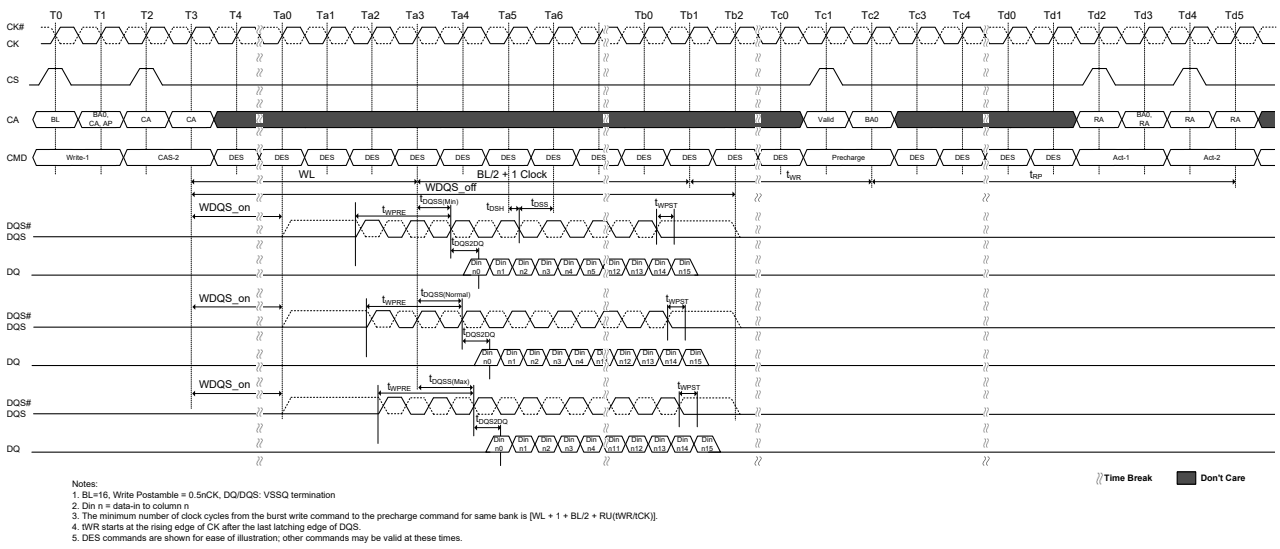
Notes:
1. BL = 16, Postamble = 1.5nCK
2. DQS and DQ terminated VSSQ
3. DQS/DQS# is “don’t care” prior to the start of tWPRE.
No transition of DQS is implied, as DQS/DQS# can be HIGH, LOW, or HI-Z prior to tWPRE.

Figure 11. DQS Write Preamble and Postamble: 1.5nCK Postamble

Burst Write Operation

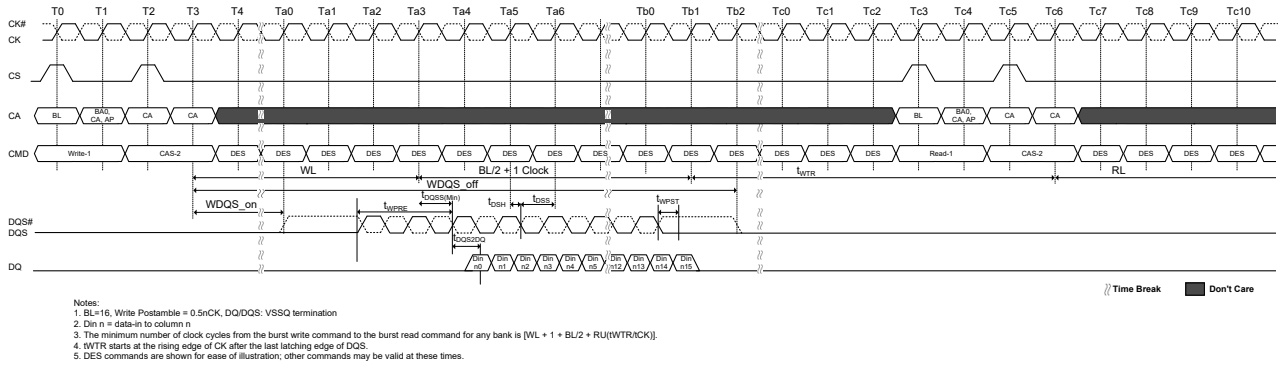
A burst Write command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for Burst Write commands, and column addresses C[1:0] are not transmitted on the CA bus (and are assumed to be zero), so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the last rising edge of the clock that completes a write command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which tDQSS is measured. The first valid “latching” edge of DQS must be driven WL * tCK + tDQSS after the rising edge of Clock that completes a write command.

The LPDDR4X-SDRAM uses an un-matched DQS-DQ path for lower power, so the DQS-strobe must arrive at the SDRAM ball prior to the DQ signal by the amount of tDQS2DQ. The DQS-strobe output is driven tWPRE before the first valid rising strobe edge. The tWPRE pre-amble is required to be 2 x tCK. The DQS strobe must be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data must be held for tDIVW (data input valid window) and the DQS must be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of DQS until the 16 or 32 bit data burst is complete. The DQS-strobe must remain active (toggling) for tWPST (Write post-amble) after the completion of the burst Write. After a burst Write operation, tWR must be satisfied before a Precharge command to the same bank can be issued. Pin input timings are measured relative to the cross point of DQS and DQS#.



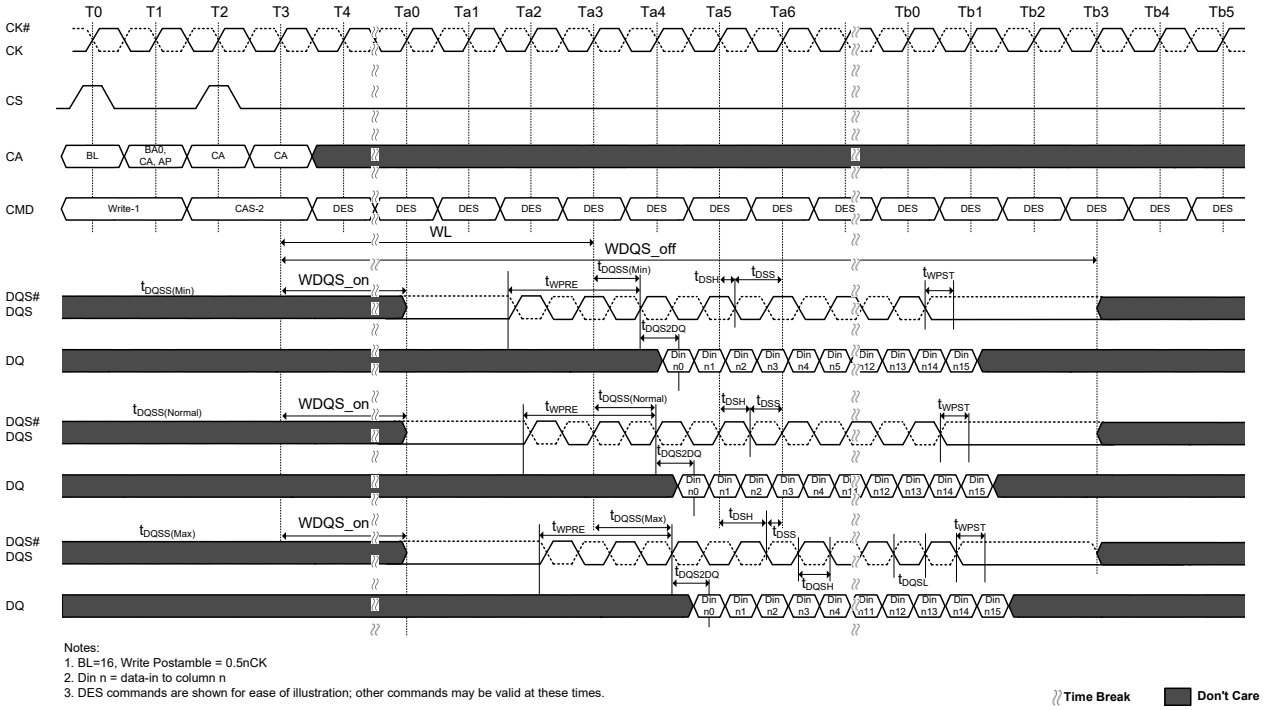
Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to column n
3. The minimum number of clock cycles from the burst write command to the precharge command for same bank is [WL + 1 + BL/2 + RU(tWR/tCK)].
4. tWR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 12. Burst Write Operation



Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to column n
3. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].
4. tWTR starts at the rising edge of CK after the last latching edge of DQS.
5. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 13. Burst Write Followed by Burst Read



Notes:
1. BL=16, Write Postamble = 0.5nCK
2. Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 14. Write Timing

Write and Masked Write operation DQS controls (WDQS Control)

LPDDR4X-SDRAMs support write and masked write operations with the following DQS controls. Before and after Write and Masked Write operations are issued, DQS/DQS# is required to have a sufficient voltage gap to make sure the write buffers operating normally without any risk of metastability.

The LPDDR4X-SDRAM is supported by either of two WDQS control modes below.
Mode 1: Read Based Control
Mode 2: WDQS_on / WDQS_off definition based control

Regardless of ODT enable/disable, WDQS related timing described here does not allow any change of existing command timing constraints for all read/write operations. In case of any conflict or ambiguity on the command timing constraints caused by the specification here, the specification defined in the Timing Constraints for Training Commands table should have higher priority than WDQS control requirements.

To prevent write preamble related failure, either of the two WDQS controls to the device should be supported.

WDQS Control Mode 1 - Read Based Control

The LPDDR4X-SDRAM needs to be guaranteed the differential WDQS, but the differential WDQS can be controlled as described below. WDQS control requirements here can be ignored while differential read DQS is operated or while DQS hands over from Read to Write and vice versa.

1. At the time a write / masked write command is issued, SoC makes the transition from driving DQS# high to driving differential DQS/DQS#, followed by normal differential burst on DQS pins.
2. At the end of post amble of write / masked write burst, SoC resumes driving DQS# high through the subsequent states except for DQS toggling and DQS turn around time of WT-RD and RD-WT as long as CKE is high.
3. When CKE is low, the state of DQS and DQS# is allowed to be “Don’t Care”.

Figure 15. WDQS Control Mode 1 - Read Based Control

WDQS Control Mode 2 - WDQS_on/off

After write / masked write command is issued, DQS and DQS# required to be differential from WDQS_on, and DQS and DQS# can be “Don’t Care” status from WDQS_off of write / masked write command. When ODT is enabled, WDQS_on and WDQS_off timing is located in the middle of the operations. When host disables ODT, WDQS_on and WDQS_off constraints conflict with tRTW. The timing does not conflict when ODT is enabled because WDQS_on and WDQS_off timing is covered in ODTLon and ODTLoff. However, regardless of ODT on/off, WDQS_on/off timing below does not change any command timing constraints for all read and write operations. In order to prevent the conflict, WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD). In addition, the period during DQS toggling caused by Read and Write can be counted as WDQS_on/off.

Parameters

- WDQS_on: the max delay from write / masked write command to differential DQS and DQS#.
- WDQS_off: the min delay for DQS and DQS# differential input after the last write / masked write command.
- WDQS_Exception: the period where WDQS_on and WDQS_off timing is overlapped with read operation or with DQS turn around (RD-WT, WT-RD).
  - WDQS_Exception @ ODT disable = max (WL - WDQS_on+ tDQSTA - tWPRE - n*tCK,0 tCK) where RD to WT command gap = tRTW(min)@ODT disable + n*tCK
  - WDQS_Exception @ ODT enable = tDQSTA

Table 11. WDQS_on / WDQS_off Definition

WL		nWR	nRTP	WDQS_on (Max)		WDQS_off (Min)		Lower Clock Frequency Limit (>)	Upper Clock Frequency Limit (≤)
Set A	Set B			Set A	Set B	Set A	Set B		
4	4	6	8	0	0	15	15	10	266
6	8	10	8	0	0	18	20	266	533
8	12	16	8	0	6	21	25	533	800
10	18	20	8	4	12	24	32	800	1066
12	22	24	10	4	14	27	37	1066	1333
14	26	30	12	6	18	30	42	1333	1600
16	30	34	14	6	20	33	47	1600	1866
18	34	40	16	8	24	36	52	1866	2133

Notes:
1. WDQS_on/off requirement can be ignored when WDQS_on/off timing is overlapped with read operation period including read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD).
2. DQS toggling period caused by read and write can be counted as WDQS_on/off.

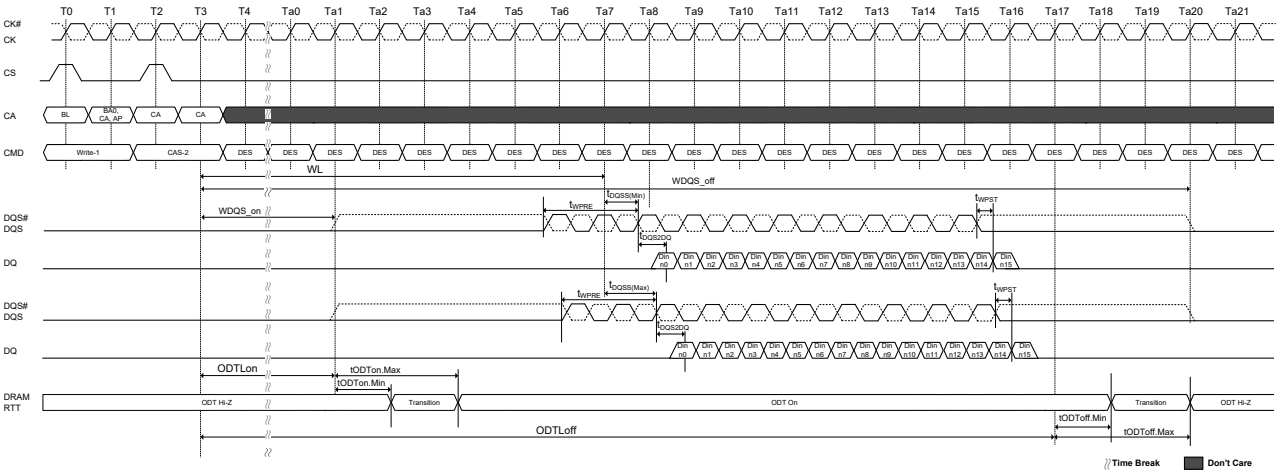
Table 12. WDQS_on / WDQS_off Allowable Variation Range

	Min	Max	Unit
WDQS_on	-0.25	0.25	tCK(avg)
WDQS_off	-0.25	0.25	tCK(avg)

Table 13. DQS turn around parameter

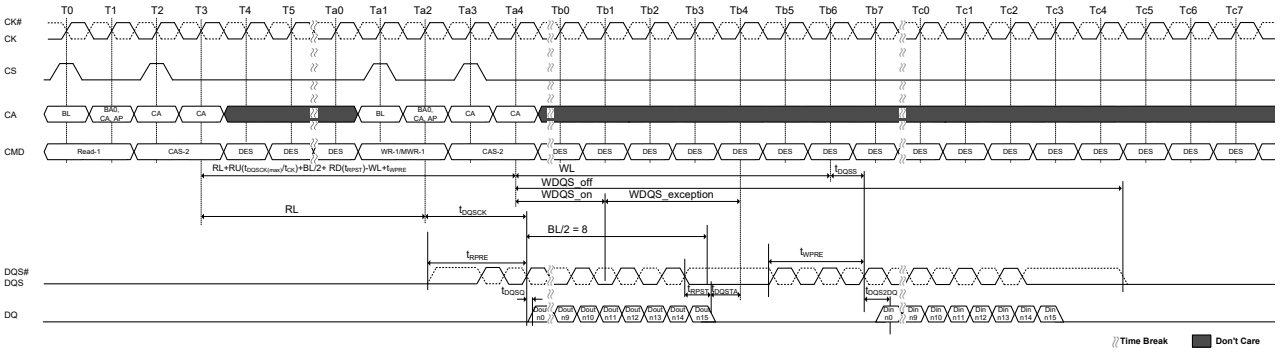
Parameter	Description	Max	Unit	Note
t_{DQSTA}	Turn-around time RDQS to WDQS for WDQS control case	0.25	tCK(avg)	1

Note 1. tDQSTA is only applied to WDQS_exception case when WDQS Control. Except for WDQS Control, tDQSTA can be ignored.



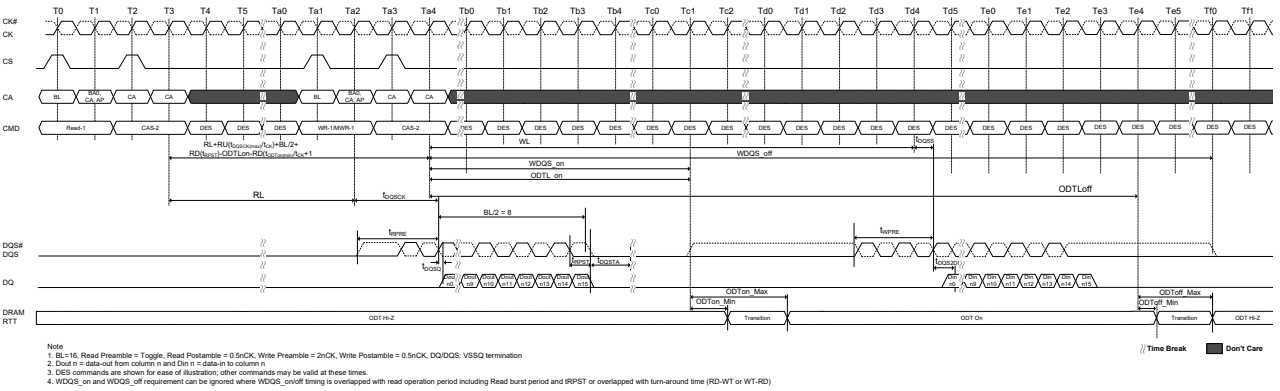
Notes:
1. BL=16, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. DRAM RTT is only applied when ODT is enabled (MR11 OP[2:0] is not 000B)

Figure 16. Burst Write Operation



Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK
2. Dout n = data-out from column n and Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD)

Figure 17. Burst Read followed by Burst Write or Burst Mask Write (ODT Disable)



Note
1. BL=16, Read Preamble = Toggle, Read Postamble = 0.5nCK, Write Preamble = 2nCK, Write Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n = data-out from column n and Din n = data-in to column n
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. WDQS_on and WDQS_off requirement can be ignored where WDQS_on/off timing is overlapped with read operation period including Read burst period and tRPST or overlapped with turn-around time (RD-WT or WT-RD)

Figure 18. Burst Read followed by Burst Write or Burst Mask Write (ODT Enable)

Multi-Purpose Command (MPC)

LPDDR4X-SDRAMs use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the SDRAM executes a NOP (no operation) command, and when OP[6]=1 then the SDRAM further decodes one of several training commands.

When OP[6]=1 and when the training command includes a Read or Write operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read or Write command. The operands of the CAS-2 command following a MPC Read/Write command must be driven LOW.

The following MPC commands must be followed by a CAS-2 command:
- Write FIFO
- Read FIFO
- Read DQ Calibration

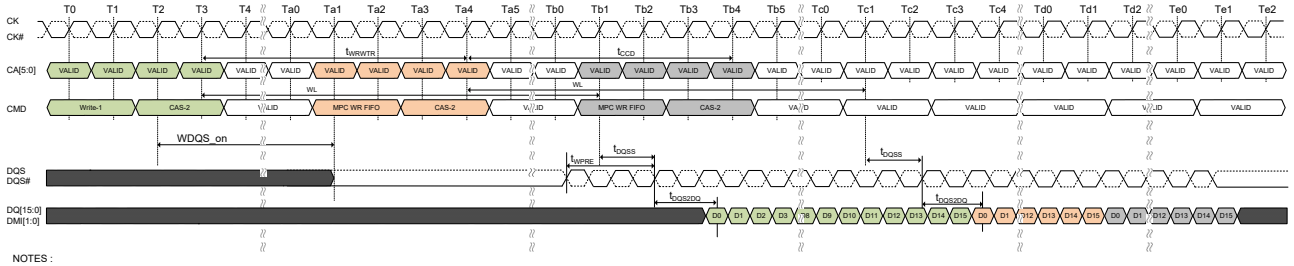
All other MPC-1 commands do not require a CAS-2 command, including:
- NOP
- Start DQS Interval Oscillator
- Stop DQS Interval Oscillator
- Start ZQ Calibration
- Latch ZQ Calibration

Table 14. MPC Command Definition

Command	Command Pins			CA Pins						CK Edge	Note
	CKE		CS	CA0	CA1	CA2	CA3	CA4	CA5		
	CK(n-1)	CK(n)									
MPC (Train, NOP)	H	H	H	L	L	L	L	L	OP6	R1	1,2
			L	OP0	OP1	OP2	OP3	OP4	OP5	R2	

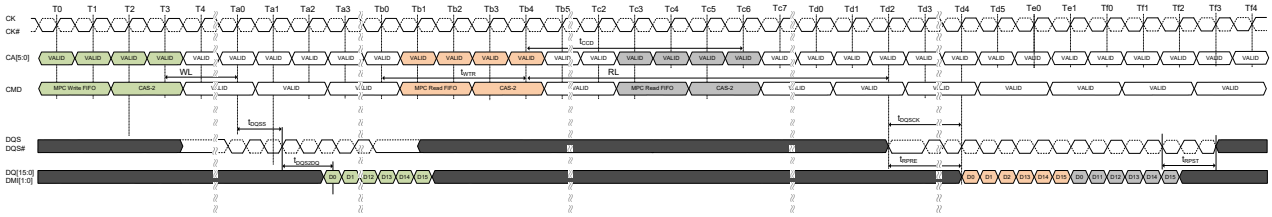
Function	Operand	Data	Note
Training Modes	OP[6:0]	0XXXXXXB: NOP 1000001B: RD FIFO: RD FIFO supports only BL16 operation 1000011B: RD DQ Calibration (MR32/MR40) 1000101B: RFU 1000111B: WR FIFO: WR FIFO supports only BL16 operation 1001001B: RFU 1001011B: Start DQS Osc 1001101B: Stop DQS Osc 1001111B: ZQCal Start 1010001B: ZQCal Latch All Others: Reserved	1,2,3

Notes:
1. See command truth table for more information.
2. MPC commands for Read or Write training operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.
3. Write FIFO and Read FIFO commands will only operate as BL16, ignoring the burst length selected by MR1 OP[1:0].



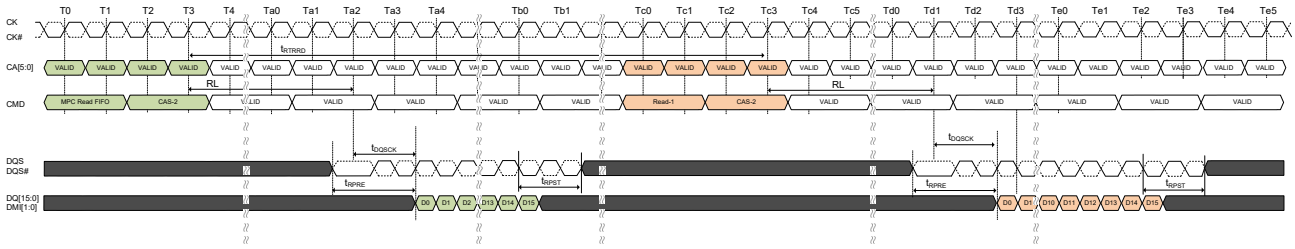
NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC [WR-FIFO] is tWRWTR.
3. Seamless MPC [WR-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [WR-FIFO] uses the same command-to-data timing relationship (WL, tDQSS, tDQS2DQ) as a Write-1 command.
5. A maximum of 5 MPC [WR-FIFO] commands may be executed consecutively without corrupting FIFO data.
   The 6th MPC [WR-FIFO] command will overwrite the FIFO data from the first command. If fewer than 5 MPC [WR-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
6. For the CAS-2 command following a MPC command, the CAS-2 operands must be driven "LOW."
7. To avoid corrupting the FIFO contents, MPC-1 [RD-FIFO] must immediately follow MPC-1 [WR-FIFO]/CAS-2 without any other command disturbing FIFO pointers in-between. FIFO pointers are disturbed by CKE Low, Write, Masked Write, Read, Read DQ Calibration and MRR. See Write Training section for more information on FIFO pointer behavior.

Figure 19. MPC [Write FIFO] Operation : tWPRE=2nCK, tWPST=0.5nCK



NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC-1 [WR-FIFO] is tWRWTR.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to The 1st FIFO and continue advancing. If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data.
   See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers.
   See Write Training section for more information on DMI behavior.

Figure 20. MPC [RD FIFO] Read Operation: tWPRE=2nCK, tWPST=0.5nCK, tRPRE=toggling, tRPST=1.5nCK



NOTES :
1. MPC [WR FIFO] can be executed with a single bank or multiple banks active, during Refresh, or during SREF with CKE HIGH.
2. MPC [RD-FIFO] to Read-1 Operation is shown as an example of command-to-command timing for MPC. Timing from MPC-1 [RD-FIFO] command to Read is tRTRRD.
3. Seamless MPC [RD-FIFO] commands may be executed by repeating the command every tCCD time.
4. MPC [RD-FIFO] uses the same command-to-data timing relationship (RL, tDQSCK) as a Read-1 command.
5. Data may be continuously read from the FIFO without any data corruption. After 5 MPC [RD-FIFO] commands the FIFO pointer will wrap back to The 1st FIFO and continue advancing.
   If fewer than 5 MPC [WR-FIFO] commands were executed, then the MPC [RD-FIFO] commands to those FIFO locations will return undefined data.
   See the Write Training section for more information on the FIFO pointer behavior.
6. For the CAS-2 command immediately following a MPC command, the CAS-2 operands must be driven "LOW."
7. DMI[1:0] signals will be driven if any of WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.

Figure 21. MPC [RD FIFO] Operation : tRPRE=toggling, tRPST=1.5nCK

Table 15. Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Unit	Note
WR/MWR	MPC [WR FIFO]	tWRWTR	nCK	1
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK)	nCK	
RD/MRR	MPC [WR FIFO]	tRTRRD	nCK	3
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	tRTRRD	nCK	3
MPC [WR FIFO]	WR/MWR	Not Allowed	-	2
	MPC [WR FIFO]	tCCD	nCK	
	RD/MRR	Not Allowed	-	2
	MPC [RD FIFO]	WL+RU(tDQSS(max)/tCK) +BL/2+RU(tWTR/tCK)	nCK	
	MPC [RD DQ Calibration]	Not Allowed	-	2
MPC [RD FIFO]	WR/MWR	tRTRRD	nCK	3
	MPC [WR FIFO]	tRTW	-	4
	RD/MRR	tRTRRD	nCK	3
	MPC [RD FIFO]	tCCD	nCK	
	MPC [RD DQ Calibration]	tRTRRD	nCK	3
MPC [RD DQ Calibration]	WR/MWR	tRTRRD	nCK	3
	MPC [WR FIFO]	tRTRRD	nCK	3
	RD/MRR	tRTRRD	nCK	3
	MPC [RD FIFO]	Not Allowed	-	2
	MPC [RD DQ Calibration]	tCCD	nCK	

Notes:

1. tWRWTR = WL + BL/2 + RU(tDQSS(max)/tCK) + max(RU(7.5ns/tCK),8nCK)
2. No commands are allowed between MPC [WR FIFO] and MPC-1 [RD FIFO] except MRW commands related to training parameters.
3. tRTRRD = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) + max(RU(7.5ns/tCK),8nCK)
4. tRTW:
   - In Case of DQ ODT Disable MR11 OP[2:0] = 000B:
     RL+RU(tDQSCK(max)/ tCK) +BL/2- WL+tWPRE+RD(tRPST)
   - In Case of DQ ODT Enable MR11 OP[2:0] ≠ 000B:
     RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) - ODTLon - RD(tODTon,min/tCK) + 1

Mode Register Definition

The table listed below shows the mode registers for LPDDR4X SDRAM. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Mode Register Assignment and Definition

Table below shows the mode registers. Each register is denoted as “R”, if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. Mode Register Read Command shall be used to read a register. Mode Register Write Command shall be used to write a register.

Table 16. Mode Register Assignments

MR#	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	Reserved	RFU	RFU	RZQI		RFU	Latency	Refresh
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
5	Reserved							
6	Reserved							
7	Reserved							
8	IO Width		Density				Type	
9	Reserved							
10	RFU							ZQ-Reset
11	DQ ODTnt	CA ODT			DQ ODTnt	DQ ODT		
12	CBT Mode	VR-CA	VREF(CA)					
13	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	RFU	VR(DQ)	VREF(DQ)					
15	Lower-Byte Invert Register for DQ Calibration							
16	PASR Bank Mask							
17	PASR Segment Mask							
18	DQS Oscillator Count - LSB							
19	DQS Oscillator Count - MSB							
20	Upper-Byte Invert Register for DQ Calibration							
21	RFU							
22	ODT for x8_2ch(Byte) mode		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		
23	DQS interval timer run time setting							
24	TRR Mode	TRR Mode BAn			Unltd MAC	MAC Value		
25	PPR Resource							
26	RFU							
27	RFU							
28	RFU							
29	RFU							
30	Reserved for testing - SDRAM will ignore							
31	RFU							
32	DQ Calibration Pattern “A” (default = 5AH)							
33	ECC control							
34	ECC error count							
35	RFU							
36	RFU							
37	RFU							
38	RFU							
39	Reserved for testing - SDRAM will ignore							
40	DQ Calibration Pattern “B” (default = 3CH)							

Table 17. MR0 Register Information (MA[5:0] = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Reserved	RFU	RFU	RZQI		RFU	Latency	Refresh

Function	Type	Operand	Data	Notes
Refresh Mode	Read-only	OP[0]	0B : Both legacy & modified refresh mode supported 1B : Only modified refresh mode supported	
Latency Mode		OP[1]	0B : Device supports normal latency 1B : Reserved	5, 6
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00B: RZQ Self-Test Not Supported 01B: ZQ pin may connect to VSSQ or float 10B: ZQ-pin may short to VDDQ 11B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to VSSQ or float, nor short to VDDQ)	1~ 4

Notes:

1. RZQI MR value, if supported, will be valid after the following sequence:
   a. Completion of MPC ZQCAL Start command to either channel.
   b. Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied.
   RZQI value will be lost after Reset.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4X-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
4. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240Ω ± 1%).
5. See byte mode addendum spec for byte mode latency details.
6. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.

Table 18. MR1 Register Information (MA[5:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00B: BL=16 Sequential (default) 01B: BL=32 Sequential 10B: BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1
WR-PRE (WR Pre-amble Length)		OP[2]	0B: Reserved 1B: WR Pre-amble = 2 x tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0B: RD Pre-amble = Static (default) 1B: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Precharge commands)		OP[6:4]	000B: nWR = 6 (default) 001B: nWR = 10 010B: nWR = 16 011B: nWR = 20 100B: nWR = 24 101B: nWR = 30 110B: nWR = 34 111B: nWR = 40	2,5,6
RPST (RD Post-Amble Length)		OP[7]	0B: RD Post-amble = 0.5 x tCK (default) 1B: RD Post-amble = 1.5 x tCK	4,5,6

Notes:

1.Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands.

2.The programmed value of nWR is the number of clock cycles the LPDDR4X-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled.

3.For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" Pre-amble.

4.OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS. The optional postamble cycle is provided for the benefit of certain memory controllers.

5.There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registersfor the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

6.There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 19. Burst Sequence for Read

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																	
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																	
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																	
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																	
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Notes:

1. C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2. The starting burst address is on 64-bit (4n) boundaries.

Table 20. Burst Sequence for Write

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																	
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Notes:

1. C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2. The starting address is on 256-bit (16n) boundaries for Burst length 16.
3. The starting address is on 512-bit (32n) boundaries for Burst length 32.
4. C2-C3 shall be set to '0' for all Write operations.

Table 21. MR2 Register Information (MA[5:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Function	Type	Operand	Data	Notes
RL (Read latency)	Write-only	OP[2:0]	**RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0B)** 000B: RL=6, nRTP = 8 (Default) 001B: RL=10, nRTP = 8 010B: RL=14, nRTP = 8 011B: RL=20, nRTP = 8 100B: RL=24, nRTP = 10 101B: RL=28, nRTP = 12 110B: RL=32, nRTP = 14 111B: RL=36, nRTP = 16 **RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1B)** 000B: RL=6, nRTP = 8 001B: RL=12, nRTP = 8 010B: RL=16, nRTP = 8 011B: RL=22, nRTP = 8 100B: RL=28, nRTP = 10 101B: RL=32, nRTP = 12 110B: RL=36, nRTP = 14 111B: RL=40, nRTP = 16	1,3,4
WL (Write latency)		OP[5:3]	**WL Set "A" (MR2 OP[6]=0B)** 000B: WL=4 (Default) 001B: WL=6 010B: WL=8 011B: WL=10 100B: WL=12 101B: WL=14 110B: WL=16 111B: WL=18 **WL Set "B" (MR2 OP[6]=1B)** 000B: WL=4 001B: WL=8 010B: WL=12 011B: WL=18 100B: WL=22 101B: WL=26 110B: WL=30 111B: WL=34	1,3,4
WLS (Write Latency Set)		OP[6]	0B: WL Set "A" (default) 1B: WL Set "B"	1,3,4
WR Lev (Write Leveling)		OP[7]	0B: Disabled (default) 1B: Enabled	2

Notes:
1. See Read and Write Latencies table for detail.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 22. MR3 Register Information (MA[5:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write-only	OP[0]	0B: VDDQ x 0.6 1B: VDDQ x 0.5 (default)	1,4
WR PST (WR Post-Amble Length)		OP[1]	0B: WR Post-amble = 0.5 x tCK (default) 1B: WR Post-amble = 1.5 x tCK (Vendor specific function)	2,3,5
Post Package Repair Protection		OP[2]	0B: PPR protection disabled (default) 1B: PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0B: Disabled (default) 1B: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	0B: Disabled (default) 1B: Enabled	2,3

Notes:

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given volt- age and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. 1.5 x tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

Table 23. MR4 Register Information (MA[5:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000B: Low temperature operating limit exceeded 001B: 4x refresh 010B: 2x refresh 011B: 1x refresh (default) 100B: 0.5x refresh 101B: 0.25x refresh, no de-rating 110B: 0.25x refresh, with de-rating 111B: High temperature operating limit exceeded	1, 2, 3, 6, 7, 8
SR Abort (Self Refresh Abort)	Write	OP[3]	0B: Disable (default) 1B: Enable	8
PPRE (Post-package repair entry/exit)	Write	OP[4]	0B: Exit PPR mode (default) 1B: Enter PPR mode	4, 8
Thermal Offset (Vender Specific Function)	Write	OP[6:5]	00B: No offset, 0~5°C gradient (default) 01B: 5°C offset, 5~10°C gradient 10B: 10°C offset, 10~15°C gradient 11B: Reserved	
TUF (Temperature Update Flag)	Read	OP[7]	0B: No change in OP[2:0] since last MR4 read (default) 1B: Change in OP[2:0] since last MR4 read	5~7

Notes:
1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. OP[2:0]=011B corresponds to a device temperature of 85 °C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1B, the device temperature is greater than 85 °C.
2. At higher temperatures (>85 °C), AC timing derating may be required. If derating is required the LPDDR4X- SDRAM will set OP[2:0]=110B.
3. The device may not operate properly when OP[2:0]=000B or 111B.
4. Post-package repair can be entered or exited by writing to OP[4].
5. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
6. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence(Te).
7. See the section on “temperature Sensor” for information on the recommended frequency of reading MR4.
8. OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.

MR5~7 (Reserved) (MA[5:0] = 05H-07H)

Table 24. MR8 Register Information (MA[5:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
IO Width		Density				Type	

Function	Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00B: S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000B: 4Gb dual channel die / 2Gb single channel die 0010B: 8Gb dual channel die / 4Gb single channel die All Others: Reserved	
IO Width		OP[7:6]	00B: x16 (per channel) All Others: Reserved	

MR9 (Reserved) (MA[5:0] = 09H)

Table 25. MR10 Register Information (MA[5:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU							ZQ-Reset

Function	Type	Operand	Data	Notes
ZQ-Reset	Write-only	OP[0]	0B: Normal Operation (Default) 1B: ZQ Reset	1, 2

Notes:
1. See ZQCal Timing Parameters for calibration latency and timing.
2. If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibra- tion commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

Table 26. MR11 Register Information (MA[5:0] = 0BH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ ODTnt	CA ODT			DQ ODTnt	DQ ODT		

Function	Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3
DQ ODTnt (DQ Bus Receiver On-Die Termination for non-target DRAM)		OP[7,3]	00B: Disable (Default) 01B: RZQ/3 10B: RZQ/5 11B: RZQ/6	1~4
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3

Notes:
1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. ODT for non-target DRAM is optional.

Table 27. MR12 Register Information (MA[5:0] = 0CH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CBT Mode	VR-CA	VREF(CA)					

Function	Type	Operand	Data	Notes
VREF(CA) (VREF(CA) Setting)	Read / Write	OP[5:0]	000000B - 110010B: See table below All Others: Reserved	1,2,3, 5,6
VR-CA (VREF(CA) Range)		OP[6]	0B: VREF(CA) Range[0] enabled 1B: VREF(CA) Range[1] enabled (default)	1,2,4, 5,6
CBT Mode	Write	OP[7]	0B: Mode1 (Default) 1B: Mode2	7

Notes:
1. This register controls the VREF(CA) levels. Refer to VREF Settings for Range[0] and Range[1] for actual voltage of VREF(CA).
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(CA) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(CA) training for more information.
4. A write to OP[6] switches the LPDDR4X-SDRAM between two internal VREF(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(CA) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
7. This field can be activated in only Byte Mode: x8. Device.

Table 28. VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDD2)		Range[1] Values (% of VDD2)		Notes
VREF Settings for MR12	OP[5:0]	000000B: 15.0%	011010B: 30.5 %	000000B: 32.9%	011010B: 48.5%	1,2,3
		000001B: 15.6%	011011B: 31.1%	000001B: 33.5%	011011B: 49.1%	
		000010B: 16.2%	011100B: 31.7%	000010B: 34.1%	011100B: 49.7%	
		000011B: 16.8%	011101B: 32.3%	000011B: 34.7%	011101B: 50.3% (default)	
		000100B: 17.4%	011110B: 32.9%	000100B: 35.3%	011110B: 50.9%	
		000101B: 18.0%	011111B: 33.5%	000101B: 35.9%	011111B: 51.5%	
		000110B: 18.6%	100000B: 34.1%	000110B: 36.5%	100000B: 52.1%	
		000111B: 19.2%	100001B: 34.7%	000111B: 37.1%	100001B: 52.7%	
		001000B: 19.8%	100010B: 35.3%	001000B: 37.7%	100010B: 53.3%	
		001001B: 20.4%	100011B: 35.9%	001001B: 38.3%	100011B: 53.9%	
		001010B: 21.0%	100100B: 36.5%	001010B: 38.9%	100100B: 54.5%	
		001011B: 21.6%	100101B: 37.1%	001011B: 39.5%	100101B: 55.1%	
		001100B: 22.2%	100110B: 37.7%	001100B: 40.1%	100110B: 55.7%	
		001101B: 22.8%	100111B: 38.3%	001101B: 40.7%	100111B: 56.3%	
		001110B: 23.4%	101000B: 38.9%	001110B: 41.3%	101000B: 56.9%	
		001111B: 24.0%	101001B: 39.5%	001111B: 41.9%	101001B: 57.5%	
		010000B: 24.6%	101010B: 40.1%	010000B: 42.5%	101010B: 58.1%	
		010001B: 25.1%	101011B: 40.7%	010001B: 43.1%	101011B: 58.7%	
		010010B: 25.7%	101100B: 41.3%	010010B: 43.7%	101100B: 59.3%	
		010011B: 26.3%	101101B: 41.9%	010011B: 44.3%	101101B: 59.9%	
		010100B: 26.9%	101110B: 42.5%	010100B: 44.9%	101110B: 60.5%	
		010101B: 27.5%	101111B: 43.1%	010101B: 45.5%	101111B: 61.1%	
		010110B: 28.1%	110000B: 43.7%	010110B: 46.1%	110000B: 61.7%	
		010111B: 28.7%	110001B: 44.3%	010111B: 46.7%	110001B: 62.3%	
		011000B: 29.3%	110010B: 44.9%	011000B: 47.3%	110010B: 62.9%	
		011001B: 29.9%	All Others: Reserved	011001B: 47.9%	All Others: Reserved	

Notes:
1. These values may be used for MR12 OP[5:0] to set the VREF(CA) levels in the LPDDR4X-SDRAM.
2. The range may be selected in the MR12 register by setting OP[6] appropriately.
3. The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high fre- quency setting which may use different terminations values.

Table 29. MR13 Register Information (MA[5:0] = 0DH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Function	Type	Operand	Data	Notes
CBT (Command Bus Training)	Write-only	OP[0]	0B: Normal Operation (default) 1B: Command Bus Training Mode Enabled	1
RPT (Read Preamble Training)		OP[1]	0B: Disable (default) 1B: Enable	
VRO (VREF Output)		OP[2]	0B: Normal operation (default) 1B: Output the VREF(CA) and VREF(DQ) values on DQ bits	2
VRCG (VREF Current Generator)		OP[3]	0B: Normal Operation (default) 1B: VREF Fast Response (high current) mode	3
RRO Refresh rate option		OP[4]	0B: Disable codes 001 and 010 in MR4 OP[2:0] 1B: Enable all codes in MR4 OP[2:0]	4, 5
DMD (Data Mask Disable)		OP[5]	0B: Data Mask Operation Enabled (default) 1B: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write/Read)		OP[6]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point [1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0B: Frequency-Set-Point[0] (default) 1B: Frequency-Set-Point [1]	8

Notes:

1. A write to set OP[0]=1 causes the LPDDR4X-SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the LPDDR4X-SDRAM will output the VREF(CA) and VREF(D) voltages on D pins. Only the “active” frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels. The DQ pins used for VREF output are vendor specific.
3. When OP[3]=1, the VREF circuit uses a high-current mode to improve VREF settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4X devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4X devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), masked write command is illegal. See LPDDR4X Data Mask (DM) and Data Bus Inversion (DBIdc) Function.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range. For more information, refer to 4.30, Frequency Set Point.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as VREF(CA) Setting, VREF(CA) Range, VREF(DQ) Setting, VREF(DQ) Range. For more information, refer to 4.30 Frequency Set Point section.

Table 30. MR14 Register Information (MA[5:0] = 0EH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU	VR(DQ)	VREF(DQ)					

Function	Type	Operand	Data	Notes
VREF(DQ) (VREF(DQ) Setting)	Read / Write	OP[5:0]	000000B - 110010B: See table below All Others: Reserved	1,2,3, 5,6
VR(DQ) (VREF(DQ) Range)		OP[6]	0B: VREF(DQ) Range[0] enabled 1B: VREF(DQ) Range[1] enabled (default)	1,2,4, 5,6

Notes:
1. This register controls the VREF(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to'0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal VREF(DQ) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for VREF(DQ) to reach the set level depends on the step size from the cur- rent level to the new level. See the section on VREF(DQ) training for more information.
4. A write to OP[6] switches the LPDDR4X-SDRAM between two internal VREF(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the VREF(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 31. VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
VREF Settings for MR14	OP[5:0]	000000B: 15.0%	011010B: 30.5 %	000000B: 32.9%	011010B: 48.5%	1,2,3
		000001B: 15.6%	011011B: 31.1%	000001B: 33.5%	011011B: 49.1%	
		000010B: 16.2%	011100B: 31.7%	000010B: 34.1%	011100B: 49.7%	
		000011B: 16.8%	011101B: 32.3%	000011B: 34.7%	011101B: 50.3% (default)	
		000100B: 17.4%	011110B: 32.9%	000100B: 35.3%	011110B: 50.9%	
		000101B: 18.0%	011111B: 33.5%	000101B: 35.9%	011111B: 51.5%	
		000110B: 18.6%	100000B: 34.1%	000110B: 36.5%	100000B: 52.1%	
		000111B: 19.2%	100001B: 34.7%	000111B: 37.1%	100001B: 52.7%	
		001000B: 19.8%	100010B: 35.3%	001000B: 37.7%	100010B: 53.3%	
		001001B: 20.4%	100011B: 35.9%	001001B: 38.3%	100011B: 53.9%	
		001010B: 21.0%	100100B: 36.5%	001010B: 38.9%	100100B: 54.5%	
		001011B: 21.6%	100101B: 37.1%	001011B: 39.5%	100101B: 55.1%	
		001100B: 22.2%	100110B: 37.7%	001100B: 40.1%	100110B: 55.7%	
		001101B: 22.8%	100111B: 38.3%	001101B: 40.7%	100111B: 56.3%	
		001110B: 23.4%	101000B: 38.9%	001110B: 41.3%	101000B: 56.9%	
		001111B: 24.0%	101001B: 39.5%	001111B: 41.9%	101001B: 57.5%	
		010000B: 24.6%	101010B: 40.1%	010000B: 42.5%	101010B: 58.1%	
		010001B: 25.1%	101011B: 40.7%	010001B: 43.1%	101011B: 58.7%	
		010010B: 25.7%	101100B: 41.3%	010010B: 43.7%	101100B: 59.3%	
		010011B: 26.3%	101101B: 41.9%	010011B: 44.3%	101101B: 59.9%	
		010100B: 26.9%	101110B: 42.5%	010100B: 44.9%	101110B: 60.5%	
		010101B: 27.5%	101111B: 43.1%	010101B: 45.5%	101111B: 61.1%	
		010110B: 28.1%	110000B: 43.7%	010110B: 46.1%	110000B: 61.7%	
		010111B: 28.7%	110001B: 44.3%	010111B: 46.7%	110001B: 62.3%	
		011000B: 29.3%	110010B: 44.9%	011000B: 47.3%	110010B: 62.9%	
		011001B: 29.9%	All Others: Reserved	011001B: 47.9%	All Others: Reserved	

Notes:
1. These values may be used for MR14 OP[5:0] to set the VREF(DQ) levels in the LPDDR4X-SDRAM.
2. The range may be selected in the MR14 register by setting OP[6] appropriately.
3. The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are pro- vided to allow for faster switching between terminated and un-terminated operation, or between different high frequency setting which may use different terminations values.

Table 32. MR15 Register Information (MA[5:0] = 0FH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Lower-Byte Invert Register for DQ Calibration							

Function	Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1,2,3

Notes:

1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combi- nation of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the “true” data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Table 33. MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

Table 34. MR16 Register Information (MA[5:0] = 10H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Bank Mask							

Function	Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0B: Bank Refresh enabled (default) : Unmasked 1B: Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes:
1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

Table 35. MR17 Register Information (MA[5:0] = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Segment Mask							

Function	Type	Operand	Data	Notes
PASR Segment Mask	Write-only	OP[7:0]	0B: Segment Refresh enabled (default) 1B: Segment Refresh disabled	

Segment	OP[n]	Segment Mask	2Gb per channel	4Gb per channel
			R13:R11	R14:R12
0	0	xxxxxxx1	000B	000B
1	1	xxxxxx1x	001B	001B
2	2	xxxxx1xx	010B	010B
3	3	xxxx1xxx	011B	011B
4	4	xxx1xxxx	100B	100B
5	5	xx1xxxxx	101B	101B
6	6	x1xxxxxx	110B	110B
7	7	1xxxxxxx	111B	111B

Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular seg- ment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.

Table 36. MR18 Register Information (MA[5:0] = 12H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count - LSB							

Function	Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	1~3

Notes:
1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

Table 37. MR19 Register Information (MA[5:0] = 13H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count - MSB							

Function	Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 MSB DRAM DQS Oscillator Count	1~3

Notes:
1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

Table 38. MR20 Register Information (MA[5:0] = 14H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-Byte Invert Register for DQ Calibration							

Function	Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55H	1,2

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combi- nation of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3- OP[6].

Table 39. MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR21 (Reserved) (MA[5:0] = 15H)

Table 40. MR22 Register Information (MA[5:0] = 16H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ODTD for x8_2ch(Byte) mode		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Function	Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000B: Disable (Default) 001B: RZQ/1 (illegal if MR3 OP[0] = 0B) 010B: RZQ/2 011B: RZQ/3 (illegal if MR3 OP[0] = 0B) 100B: RZQ/4 101B: RZQ/5 (illegal if MR3 OP[0] = 0B) 110B: RZQ/6 (illegal if MR3 OP[0] = 0B) 111B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non- terminating rank)		OP[3]	ODT bond PAD is ignored 0B: ODT-CK Enable (Default) 1B: ODT-CK Disable	2,3,4
ODTE-CS (CS ODT enable for non- terminating rank)		OP[4]	ODT bond PAD is ignored 0B: ODT-CS Enable (Default) 1B: ODT-CS Disable	2,3,4
ODTD-CA (CA ODT termination disable)		OP[5]	ODT bond PAD is ignored 0B: ODT-CA Enable (Default) 1B: ODT-CA Disable	2,3,4
x8ODTD[7:0] (CA/CLK ODT termination disable, [7:0] Byte select)		OP[6]	Byte mode device x8 2ch only, upper [15:8] Byte selected Device 0B: ODT-CS/CA/CLK follows MR11 OP[6:4] and MR22 OP[5:3] (default) 1B: ODT-CS/CA/CLK Disabled	4
x8ODTD[7:0] (CA/CLK ODT termination disable, [15:8] Byte select)		OP[7]	Byte mode device x8 2ch only, upper [15:8] Byte selected Device 0B: ODT-CS/CA/CLK follows MR11 OP[6:4] and MR22 OP[5:3] (default) 1B: ODT-CS/CA/CLK Disabled	4

Notes:

1. All values are “typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. The ODT_CA pin is ignored by LPDDR4X devices. The ODT_CA pin shall be connected to either VDD2 or VSS. CA/ CS/ CK ODT is fully controlled through MR11 and MR22. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed.

Table 41. MR23 Register Information (MA[5:0] = 17H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run time setting							

Function	Type	Operand	Data	Notes
DQS interval timer run time	Write-only	OP[7:0]	00000000B: DQS interval timer stop via MPC Command (Default) 00000001B: DQS timer stops automatically at 16th clocks after timer start 00000010B: DQS timer stops automatically at 32nd clocks after timer start 00000011B: DQS timer stops automatically at 48th clocks after timer start 00000100B: DQS timer stops automatically at 64th clocks after timer start ------- Thru ------- 00111111B: DQS timer stops automatically at (63X16) th clocks after timer start 01XXXXXXB: DQS timer stops automatically at 2048th clocks after timer start 10XXXXXXB: DQS timer stops automatically at 4096th clocks after timer start 11XXXXXXB: DQS timer stops automatically at 8192nd clocks after timer start	1,2

Notes:
1. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000B.
2. MPC command with OP[6:0]=1001101B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

Table 42. MR24 Register Information (MA[5:0] = 18H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR Mode	TRR Mode BAn			Unltd MAC	MAC Value		

Function	Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	000B: Unknown when bit OP3=0 (Note 1) Unlimited when bit OP3=1 (Note 2) 001B: 700K 010B: 600K 011B: 500K 100B: 400K 101B: 300K 110B: 200K 111B: Reserved	
Unlimited MAC		OP[3]	0B: OP[2:0] define MAC value 1B: Unlimited MAC value (Note 2, Note 3)	
TRR Mode BAn	Write-only	OP[6:4]	000B: Bank 0 001B: Bank 1 010B: Bank 2 011B: Bank 3 100B: Bank 4 101B: Bank 5 110B: Bank 6 111B: Bank 7	
TRR Mode		OP[7]	0B: Disabled (default) 1B: Enabled	

Notes:
1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

Table 43. MR25 Register Information (MA[5:0] = 19H)

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank7	Bank6	Bank5	Bank4	Bank3	Bank2	Bank1	Bank0

Function	Type	Operand	Data
PPR Resource	Read-only	OP[2:0]	0B: PPR Resource is not available 1B: PPR Resource is available

MR26~29 (Reserved) (MA[5:0] = 1AH-1DH)

Table 44. MR30 Register Information (MA[5:0] = 1EH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR31 (Reserved) (MA[5:0] = 1FH)

Table 45. MR32 Register Information (MA[5:0] = 20H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern “A” (default = 5AH)							

Function	Type	Operand	Data
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	XB: An MPC command with OP[6:0]= 1000011B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern “5AH”is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)

Table 46. MR33 Register Information (MA[5:0] = 21H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ECCON	ERRON	CLR ECC	RFU			ECC 2err	ECC Event

Function	Type	Operand	Data
ECCON	Read / Write	OP[7]	0: ECC function off 1: ECC function on(default)
ERRON	Read / Write	OP[6]	0: ECC ERR info output through ECC pad function off(default) 1: ECC ERR info output through ECC pad function on
CLR ECC	Write-only	OP[5]	0: ECC Event Record Clear off(default) 1: ECC Event Record Clear on
ECC 2err	Read-only	OP[1]	0: No 2bit err 1: 2bit err detect
ECC Event	Read-only	OP[0]	0: No ECC event 1: ECC Event detect

Bit “ERRON”(op6) is valid only if bit “ECCON”(bit7) is valid first.
Bit “CLR ECC”(op5) is self clean and will clear both “ECC 2err”(op1) and “ECC Event”(op0) if it is write with “1”.
Bit “ECC 2err” and “ECC Event” will keep error status valid once set by ECC err information until “CLR ECC” bit sent.

Table 47. MR34 Register Information (MA[5:0] = 22H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
ECC event Number							

Function	Type	Operand	Data
ECC event Number	Read-only	OP[7:0]	00000000B: No ECC event detect 00000001B: 1 time ECC event detect 00000010B: 2 times ECC event detect 00000011B: 3 times ECC event detect . . . 11111111B: 255 times ECC event detect

The ecc event number will hold max value (0xFF) if it is overflow. And it can also be cleared by MR33 bit “CLR ECC”.

MR35~38 (Reserved) (MA[5:0] = 21H-26H)

Table 48. MR39 Register Information (MA[5:0] = 27H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:

1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

Table 49. MR40 Register Information (MA[5:0] = 28H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern “B” (default = 3CH)							

Function	Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write-only	OP[7:0]	XB: A default pattern “3CH” is loaded at power- up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3

Notes:

1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized “little endian” such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H , then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

Table 50. Refresh Requirement Parameters per die for Dual Channel devices

Refresh Requirements		Symbol	128Mx32 (4Gb/Package)	Units
Density per Channel			2Gb	
Number of banks per channel			8	
Refresh Window (tREFW) (TCASE ≤ 85°C) (1x Refresh)[2,3]		tREFW	32	ms
Refresh Window (tREFW) (1/2 Rate Refresh)		tREFW	16	ms
Refresh Window (tREFW) (1/4 Rate Refresh)		tREFW	8	ms
Required Number of REFRESH Commands in a tREFW window		R	8192	-
Average Refresh Interval (1x Refresh)[2]	REFAB	tREFI	3.904	us
	REFPB	tREFIpb	488	ns
Refresh Cycle Time (All Banks)		tRFCab	130	ns
Refresh Cycle Time (Per Bank)		tRFCpb	60	ns

Notes:

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. 1x refersh rate (tREFW=32ms) is supported at all temperatures at or below 85°C Tcase. If MR4 OP[2:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.
3. Refer to MR4 OP[2:0] for detailed Refresh Rate and its multipliers.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 51. Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units	Notes
VDD1	VDD1 supply voltage relative to Vss	-0.4	2.1	V	1
VDD2	VDD2 supply voltage relative to Vss	-0.4	1.5	V	1
VDDQ	VDDQ supply voltage relative to VSSQ	-0.4	1.5	V	1
VIN, VOUT	Voltage on any ball except VDD1 relative to Vss	-0.4	1.5	V	
TSTG	Storage Temperature	-55	125	℃	2

Notes:
1. See “Power-Ramp” for relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the LPDDR4X device. For the mea- surement conditions, please refer to JESD51-2.

Table 52. Operating Temperature Range

Symbol	Parameter	Min	Max	Units	Notes
TOPER	Standard	-40	85	℃	1~3

Notes:
1. Operating Temperature is the case surface temperature on the center-top side of the device. For the measurement conditions, please refer to JESD51-2.
2. Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.
3. Refer to operating temperature range on first page.

AC and DC Operating Conditions

Table 53. Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD1	Core 1 Power	1.70	1.80	1.95	V	1,2
VDD2	Core 2 Power/Input Buffer Power	1.06	1.10	1.17	V	1,2,3
VDDQ	I/O Buffer Power	0.57	0.6	0.65	V	2,3,4,5

Notes:
1. VDD1 uses significantly less current than VDD2.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20MHz.
4. VDDQ(max) may be extended to 0.67 V as an option in case the operating clock frequency is equal or less than 800 Mhz.
5. Pull up, pull down and ZQ calibration tolerance spec is valid only in normal VDDQ tolerance range (0.57 V - 0.65 V).

Table 54. Input Leakage Current

Symbol	Parameter	Min	Max	Units	Notes
IL	Input Leakage current	-4	4	uA	1,2

Notes:

1. For CK, CK#, CKE, CS, CA, ODT_CA and RESET#. Any input 0V≦VIN≦VDD2 (All other pins not under test = 0V).
2. CA ODT is disabled for CK, CK#, CS, and CA.

Table 55. Input/Output Leakage Current

Symbol	Parameter	Min	Max	Units	Notes
IOZ	Input/Output Leakage current	-5	5	uA	1,2

Notes:

1. For DQ, DQS, DQS# and DMI. Any I/O 0V ≦ VOUT ≦ VDDQ.
2. I/Os status are disabled: High Impedance and ODT Off.

Table 56. Input/output capacitance

Symbol	Parameter	Min	Max	Units	Notes
CCK	Input capacitance, CK and CK#	0.5	0.9	pF	1,2
CDCK	Input capacitance delta, CK and CK#	0.0	0.09	pF	1,2,3
CI	Input capacitance, All other input-only pins	0.5	0.9	pF	1,2,4
CDI	Input capacitance delta, All other input-only pins	-0.1	0.1	pF	1,2,5
CIO	Input/output capacitance, DQ, DMI, DQS, DQS#	0.7	1.3	pF	1,2,6
CDDQS	Input/output capacitance delta, DQS,DQS#	0.0	0.1	pF	1,2,7
CDIO	Input/output capacitance delta, DQ, DMI	-0.1	0.1	pF	1,2,8
CZQ	Input/output capacitance, ZQ pin	0.0	5.0	pF	1,2

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK, CCK#.
4. CI applieds to CS, CKE, CA0~CA5.
5. CDI = CI - 0.5 x (CCK + CCK#)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS and CDQS#.
8. CDIO = CIO - 0.5 x (CDQS + CDQS#) in byte-lane.

Table 57. Read and Write Latencies

Read Latency		Write Latency		nWR	nRTP	Lower Clock Frequency Limit [MHz](>)	Upper Clock Frequency Limit [MHz](≦)	Notes
No DBI	w/DBI	Set A	Set B					
6	6	4	4	6	8	10	266	1,2,3, 4,5,6
10	12	6	8	10	8	266	533	
14	16	8	2	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	-	

Notes:

1. The device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3 OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set “A” and Set "B" is determined by MR2 OP[6]. When MR2 OP[6]=0, then Write Latency Set "A" should be used. When MR2 OP[6]=1，then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Pre- charge). It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (Auto Pre- charge). It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

Asynchronous ODT

The ODT Mode is enabled if MR11 OP[3:0] are non-zero. In this case, the value of RTT is determined by the settings of those bits.

The ODT Mode is disabled if MR11 OP[3] = 0.

Table 58. ODTLon and ODTLoff Latency

ODTLon Latency[1]		ODTLoff Latency[2]		Lower Clock Frequency Limit [MHz] (>)	Upper Clock Frequency Limit [MHz] (≦)
tWPRE = 2tCK					
WL Set "A"	WL Set "B"	WL Set "A"	WL Set "B"		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	-

Notes:
1. ODTLon is referenced from CAS-2 command.
2. ODTLoff as shown in table assumes BL=16. For BL32, 8 tCK should be added.

The ODT Mode for non-target DRAM ODT control is enabled if MR11 OP[7,3] is set to a non-zero value. The ODT Mode for non-target DRAM is disabled if MR11 OP[7,3] = 00B.

Table 59. ODTLon_rd and ODTLoff_rd Latency Values (MR0 [OP1=0])

ODTLon_rd Latency		ODTLoff_rd Latency[1,2]		Lower Clock Frequency Limit [MHz] (>)	Upper Clock Frequency Limit [MHz](≦)
No DBI	w/DBI	No DBI	w/ DBI		
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	N/A	N/A	N/A	533	800
14	16	32	34	800	1066
18	22	36	40	1066	1333
22	26	42	46	1333	1600
26	30	46	50	1600	-

Notes:
1. ODTLoff_rd assumes BL=16, For BL32, 8tCK should be added.
2. ODTLoff_rd assumes a fixed tRPST of 1.5tCK.

Table 60. IDD and IDDQ Specification Parameters (3200Mbps)

(T_{OPER}, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V, V_{DD2} = 1.06-1.17V)

Parameter	Supply	128Mx32 (4Gb/Package)	Unit
IDD01	VDD1	18	mA
IDD02	VDD2	79	mA
IDD0Q	VDDQ	0.5	mA
IDD2P1	VDD1	1.2	mA
IDD2P2	VDD2	2.5	mA
IDD2PQ	VDDQ	0.3	mA
IDD2PS1	VDD1	1.2	mA
IDD2PS2	VDD2	2.5	mA
IDD2PSQ	VDDQ	0.3	mA
IDD2N1	VDD1	1.5	mA
IDD2N2	VDD2	35	mA
IDD2NQ	VDDQ	0.3	mA
IDD2NS1	VDD1	1.5	mA
IDD2NS2	VDD2	25	mA
IDD2NSQ	VDDQ	0.3	mA
IDD3P1	VDD1	1.5	mA
IDD3P2	VDD2	15	mA
IDD3PQ	VDDQ	0.3	mA
IDD3PS1	VDD1	1.5	mA
IDD3PS2	VDD2	15	mA
IDD3PSQ	VDDQ	0.3	mA
IDD3N1	VDD1	2	mA
IDD3N2	VDD2	45	mA
IDD3NQ	VDDQ	0.5	mA
IDD3NS1	VDD1	2	mA
IDD3NS2	VDD2	45	mA
IDD3NSQ	VDDQ	0.5	mA
IDD4R1	VDD1	3	mA
IDD4R2	VDD2	500	mA
IDD4RQ	VDDQ	300	mA
IDD4W1	VDD1	3	mA
IDD4W2	VDD2	400	mA
IDD4WQ	VDDQ	3	mA
IDD51	VDD1	50	mA
IDD52	VDD2	120	mA
IDD5Q	VDDQ	0.5	mA
IDD5AB1	VDD1	10	mA
IDD5AB2	VDD2	53	mA
IDD5ABQ	VDDQ	0.5	mA
IDD5PB1	VDD1	10	mA
IDD5PB2	VDD2	53	mA
IDD5PBQ	VDDQ	0.5	mA

Table 61. IDD6 specification (3200Mbps)

(T_{OPER}, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V, V_{DD2} = 1.06-1.17V)

Temperature	Parameter	Supply	128Mx32 (4Gb/Package)	Unit
45°C	IDD61	VDD1	2.5	mA
	IDD62	VDD2	4	mA
	IDD6Q	VDDQ	0.5	mA
85°C	IDD61	VDD1	7.5	mA
	IDD62	VDD2	13	mA
	IDD6Q	VDDQ	0.5	mA

Electrical Characteristics and AC Timing

Table 62. AC Timing (T_{OPER}, V_{DDQ} = 0.57-0.65V, V_{DD1} = 1.70-1.95V, V_{DD2} = 1.06-1.17V)

Symbol	Parameter	Data Rate				Unit
		2400		3200		
		Min.	Max.	Min.	Max.	
Clock Timing						
$t_{CK(avg)}$	Average clock period	0.833	100	0.625	100	ns
$t_{CH(avg)}$	Average High pulse width	0.46	0.54	0.46	0.54	t_{CK}
$t_{CL(avg)}$	Average Low pulse width	0.46	0.54	0.46	0.54	t_{CK}
$t_{CK(abs)}$	Absolute clock period	**Min:** $t_{CK(avg)min}$ + $t_{JIT(per),min}$				ns
$t_{CH(abs)}$	Absolute High clock pulse width	0.43	0.57	0.43	0.57	t_{CK}
$t_{CL(abs)}$	Absolute Low clock pulse width	0.43	0.57	0.43	0.57	t_{CK}
$t_{JIT(per)}$	Clock period jitter	-50	50	-40	40	ps
$t_{JIT(cc)}$	Maximum Clock Jitter between consecutive cycles	-	100	-	80	ps
Core Parameters						
t_{RC}	Activate-to-Activate command period (same bank)	**Min:** t_{RAS} + t_{RPab} (with all bank precharge) t_{RAS} + t_{RPpb} (with per bank precharge)				ns
t_{SR}	Minimum Self Refresh Time (Entry to Exit)	max(15ns, 3nCK)	-	max(15ns, 3nCK)	-	ns
t_{XSR}	Self Refresh exit to next valid command delay	max(t_{RFCab} + 7.5ns, 2nCK)	-	max(t_{RFCab} + 7.5ns, 2nCK)	-	ns
t_{XP}	Exit Power-Down to next valid command delay	max(7.5ns, 5nCK)	-	max(7.5ns, 5nCK)	-	ns
t_{CCD}	CAS-to-CAS delay	8	-	8	-	t_{CK}
t_{RTP}	Internal Read to Preaharge command delay	max(7.5ns, 8nCK)	-	max(7.5ns, 8nCK)	-	ns
t_{RCD}	RAS-to-CAS delay	max(18ns, 4nCK)	-	max(18ns, 4nCK)	-	ns
t_{RPpb}	Row precharge time (single bank)	max(18ns, 4nCK)	-	max(18ns, 4nCK)	-	ns
t_{RPab}	Row precharge time (all banks)	max(21ns, 4nCK)	-	max(21ns, 4nCK)	-	ns
t_{RAS}	Row active time	**Min:** max(42ns, 3nCK) **Max:** Min(9 x t_{REFI} x Refresh Rate, 70.2) us (Refresh Rate is specified by MR4, OP[2:0])				ns
t_{WR}	Write recovery time	max(18ns, 6nCK)	-	max(18ns, 6nCK)	-	ns
t_{WTR}	Write-to-Read delay	max(10ns, 8nCK)	-	max(10ns, 8nCK)	-	ns
t_{RRD}	Active bank-A to active bank-B	max(10ns, 4nCK)	-	max(10ns, 4nCK)	-	ns
t_{PPD}[1,2]	Precharge to Precharge Delay	4	-	4	-	t_{CK}
t_{FAW}	Four-bank Activate window	40	-	40	-	ns
Read output timings[3] (Unit UI = tCK(avg)min/2)						
t_{DQSQ}	DQS,DQS# to DQ Skew total, per group,per access (DBI-Disabled)	-	0.18	-	0.18	UI
t_{QH}[5]	DQ output hold time total from DQS, DQS# (DBI Disabled)	min(t_{QSH}, t_{QSL})	-	min(t_{QSH}, t_{QSL})	-	UI
t_{QW_total}[4,5]	DQ output window timetotal, per pin (DBI-Disabled)	0.73	-	0.7	-	UI
t_{QW_dj}	DQ output window timedeterministic, per pin (DBI-Disabled)	TBD	-	TBD	-	UI
t_{DQSQ_DBI}	DQS,DQS# to DQSkew total,per group,per access (DBI-Enabled)	-	0.18	-	0.18	UI
t_{QH_DBI}	DQ output hold time total from DQS, DQS# (DBI-Enabled)	min (t_{QSH_DBI}, t_{QSL_DBI})	-	min (t_{QSH_DBI}, t_{QSL_DBI})	-	UI
$t_{QW_total_DBI}$[5]	DQ output window timetotal, per pin (DBI-Enabled)	0.73	-	0.70	-	UI
t_{QSL}[5,6]	DQS, DQS# differential output low time (DBI-Disabled)	$t_{CL(abs)}$ -0.05	-	$t_{CL(abs)}$ -0.05	-	t_{CK}

t_{QSH}[5,7]	DQS, DQS# differential output high time (DBI-Disabled)	$t_{CH(abs)}$ -0.05	-	$t_{CH(abs)}$ -0.05	-	t_{CK}
t_{QSL_DBI}[6,7]	DQS, DQS# differential output low time (DBI-Enabled)	$t_{CL(abs)}$ -0.045	-	$t_{CL(abs)}$ -0.045	-	t_{CK}
t_{QSH_DBI}[7,8]	DQS, DQS# differential output high time (DBI-Enabled)	$t_{CH(abs)}$ -0.045	-	$t_{CH(abs)}$ -0.045	-	t_{CK}
Read AC Timing						
t_{RPRE}	Read preamble	1.8	-	1.8	-	t_{CK}
t_{RPST}	0.5 tCK Read postamble	0.4	-	0.4	-	t_{CK}
t_{RPST}	1.5 tCK Read postamble	1.4	-	1.4	-	t_{CK}
$t_{LZ(DQ)}$	DQ low-impedance time from CK, CK#	**Min:** (RL x t_{CK}) + $t_{DQSCK(Min)}$ - 200ps				ps
$t_{HZ(DQ)}$	DQ high impedance time from CK, CK#	**Max:** (RL x t_{CK}) + $t_{DQSCK(Max)}$ + $t_{DQSQ(Max)}$ + (BL/2xt_{CK})-100ps				ps
$t_{LZ(DQS)}$	DQS# low-impedance time from CK, CK#	**Min:** (RL x t_{CK}) + $t_{DQSCK(Min)}$ -($t_{RPRE(Max)}$ x t_{CK}) - 200ps				ps
$t_{HZ(DQS)}$	DQS# high impedance time from CK, CK#	**Max:** (RL x t_{CK}) + $t_{DQSCK(Max)}$ +(BL/2 x t_{CK}) + ($t_{RPST(Max)}$ x t_{CK}) - 100ps				ps
t_{DQSQ}	DQS-DQ skew	-	0.18	-	0.18	UI
tDQSCK Timing						
t_{DQSCK}[9]	DQS Output Access Time from CK/CK#	1.5	3.5	1.5	3.5	ns
t_{DQSCK_temp}[10]	DQS Output Access Time from CK/CK# - Temperature Variation	-	4	-	4	ps/°C
t_{DQSCK_volt}[11]	DQS Output Access Time from CK/CK# - Voltage Variation	-	7	-	7	ps/mV
$t_{DQSCK_rank2rank}$	CK to DQS Rank to Rank variation[12,13]	-	1.0	-	1.0	ns
Timing DRAM DQs In Receive Mode (Unit UI = tCK(avg)min/2)						
V_{dIVW_total}	Rx Mask voltage - p-p total[14~17]	-	140	-	140	mV
T_{dIVW_total}	Rx timing window total (At VdlVW voltage levels)[14,15,17]	-	0.22	-	0.25	UI
T_{dIVW_1bit}	Rx timing window 1 bit toggle (At VdlVW voltage levels)[14,15,17,25]	-	TBD	-	TBD	UI
V_{IHL_AC}	DQ AC input pulse amplitude pk-pk[18,26]	180	-	180	-	mV
$T_{dIPW\ DQ}$	Input pulse width (At Vcent_DQ)[19]	0.45		0.45		UI
t_{DQS2DQ}	DQ to DQS offset[20]	200	800	200	800	ps
t_{DQ2DQ}	DQ to DQ offset[21]	-	30	-	30	ps
t_{DQS2DQ_temp}	DQ to DQS offset temperature variation[22]	-	0.6	-	0.6	ps/°C
t_{DQS2DQ_volt}	DQ to DQS offset voltage variation[23]	-	33	-	33	ps/ 50mV
S_{RIN_dIVW}	Input Slew Rate over VdlVWJotal[24]	1	7	1	7	V/ns
$t_{DQS2DQ_rank2rank}$	DQ to DQS offset rank to rank variation[27,28]	-	200	-	200	ps
Write AC Timing						
t_{DQSS}	Write command to 1st DQS latching	0.75	1.25	0.75	1.25	t_{CK}
t_{DQSH}	DQS input high-level	0.4	-	0.4	-	t_{CK}
t_{DQSL}	DQS input low-level width	0.4	-	0.4	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time	0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK	0.2	-	0.2	-	t_{CK}
t_{WPRE}	Write preamble	1.8	-	1.8	-	t_{CK}
t_{WPST}[29]	0.5 tCK Write postamble	0.4	-	0.4	-	t_{CK}
t_{WPST}[29]	1.5 tCK Write postamble	1.4	-	1.4	-	t_{CK}
Power-Down AC Timing						
t_{CKE}	CKE minimum pulse width (HIGH and LOW pulse width)	Max(7.5ns, 4nCK)	-	Max(7.5ns, 4nCK)	-	ns
t_{CMDCKE}[30]	Delay from valid command to CKE input LOW	Max(1.75ns, 3nCK)	-	Max(1.75ns, 3nCK)	-	ns
t_{CKELCK}[30]	Valid Clock Requirement after CKE Input low	Max(5ns, 5nCK)	-	Max(5ns, 5nCK)	-	ns
t_{CSCKE}	Valid CS Requirement before CKE Input Low	1.75	-	1.75	-	ns

t_{CKELCS}	Valid CS Requirement after CKE Input low	Max(5ns, 5nCK)	-	Max(5ns, 5nCK)	-	ns
t_{CKCKEH}[30]	Valid Clock Requirement before CKE Input High	Max(1.75ns, 3nCK)	-	Max(1.75ns, 3nCK)	-	ns
t_{XP}[30]	Exit power- down to next valid command delay	Max(7.5ns, 5nCK)	-	Max(7.5ns, 5nCK)	-	ns
t_{CSCKEH}	Valid CS Requirement before CKE Input High	1.75	-	1.75	-	ns
t_{CKEHCS}	Valid CS Requirement after CKE Input High	Max(7.5ns, 5nCK)	-	Max(7.5ns, 5nCK)	-	ns
$t_{MRWCKEL}$[30]	Valid Clock and CS Requirement after CKE Input low after MRW Command	Max(14ns, 10nCK)	-	Max(14ns, 10nCK)	-	ns
t_{ZQCKE}[30]	Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	Max(1.75ns, 3nCK)	-	Max(1.75ns, 3nCK)	-	ns
Command Address Input Parameters (Unit UI = tCK(avg)min/2)						
V_{CIVW}[31~33]	Rx Mask voltage - p-p	-	-	-	155	mV
T_{CIVW}[31~33]	Rx timing window	-	-	-	0.3	UI
V_{IHL_AC}[34,37]	CA AC input pulse amplitude pk-pk	-	-	190	-	mV
T_{CIPW}[35]	CA input pulse width	-	-	0.6		UI
S_{RIN_CIVW}[36]	Input Slew Rate over VcIVW	-	-	1	7	V/ns
Mode Register Read/Write AC timing						
t_{MRRI}	Additional time after t_{XP} has expired until MRR command may be issued	t_{RCD} + 3nCK	-	t_{RCD} + 3nCK	-	-
t_{MRR}	Mode Register Read command period	8	-	8	-	nCK
t_{MRW}	Mode Register Write command period	max(10ns, 10nCK)	-	max(10ns, 10nCK)	-	-
t_{MRD}	Mode register set command delay	max(14ns, 10nCK)	-	max(14ns, 10nCK)	-	-
Asynchronous ODT iming						
t_{ODTon}	Asynchronous ODT Turn On	1.5	3.5	1.5	3.5	ns
t_{ODToff}	Asynchronous ODT Turn Off	1.5	3.5	1.5	3.5	ns
Self-Refresh Timing Parameters						
t_{ESCKE}[38]	Delay from SRE command to CKE Input low	max(1.75ns, $3t_{CK}$)	-	max(1.75ns, $3t_{CK}$)	-	ns
t_{SR}[38]	Minimum Self Refresh Time	max(15ns, $3t_{CK}$)	-	max(15ns, $3t_{CK}$)	-	ns
t_{XSR}[38,39]	Exit Self Refresh to Valid commands	max(t_{RFCab} + 7.5ns, $2t_{CK}$)	-	max(t_{RFCab} + 7.5ns, $2t_{CK}$)	-	ns
Command Bus Training AC Timing						
t_{CKELCK}	Valid Clock Requirement after CKE Input low	max(5ns, 5nCK)	-	max(5ns, 5nCK)	-	-
$t_{DStrain}$	Data Setup for VREF Training Mode	2	-	2	-	ns
$t_{DHtrain}$	Data Hold for VREF Training Mode	2	-	2	-	ns
t_{ADR}	Asynchronous Data Read	-	20	-	20	ns
t_{CACD}[41]	CA Bus Training Command to CA Bus Training Command Delay	RU(t_{ADR}/t_{CK})	-	RU(t_{ADR}/t_{CK})	-	t_{CK}
t_{DQSCKE}[40]	Valid Strobe Requirement before CKE Low	10	-	10	-	ns
t_{CAENT}	First CA Bus Training Command Following CKE Low	250	-	250	-	ns
t_{VREFCA_LONG}	VREF Step Time – multiple steps	-	250	-	250	ns
t_{VREFCA_SHORT}	Vref Step Time -one step	-	80	-	80	ns
$t_{CKPRECS}$	Valid Clock Requirement before CS High	$2t_{CK}$ + t_{XP} (t_{XP} = max(7.5ns, 5nCK))	-	$2t_{CK}$ + t_{XP} (t_{XP} = max(7.5ns, 5nCK))	-	-
$t_{CKPSTCS}$	Valid Clock Requirement after CS High	max(7.5ns, 5nCK))	-	max(7.5ns, 5nCK))	-	-
t_{CS_VREF}	Minimum delay from CS to DQS toggle in command bus training	2	-	2	-	t_{CK}
$t_{CKEHDQS}$	Minimum delay from CKE High to Strobe High Impedance	10				ns

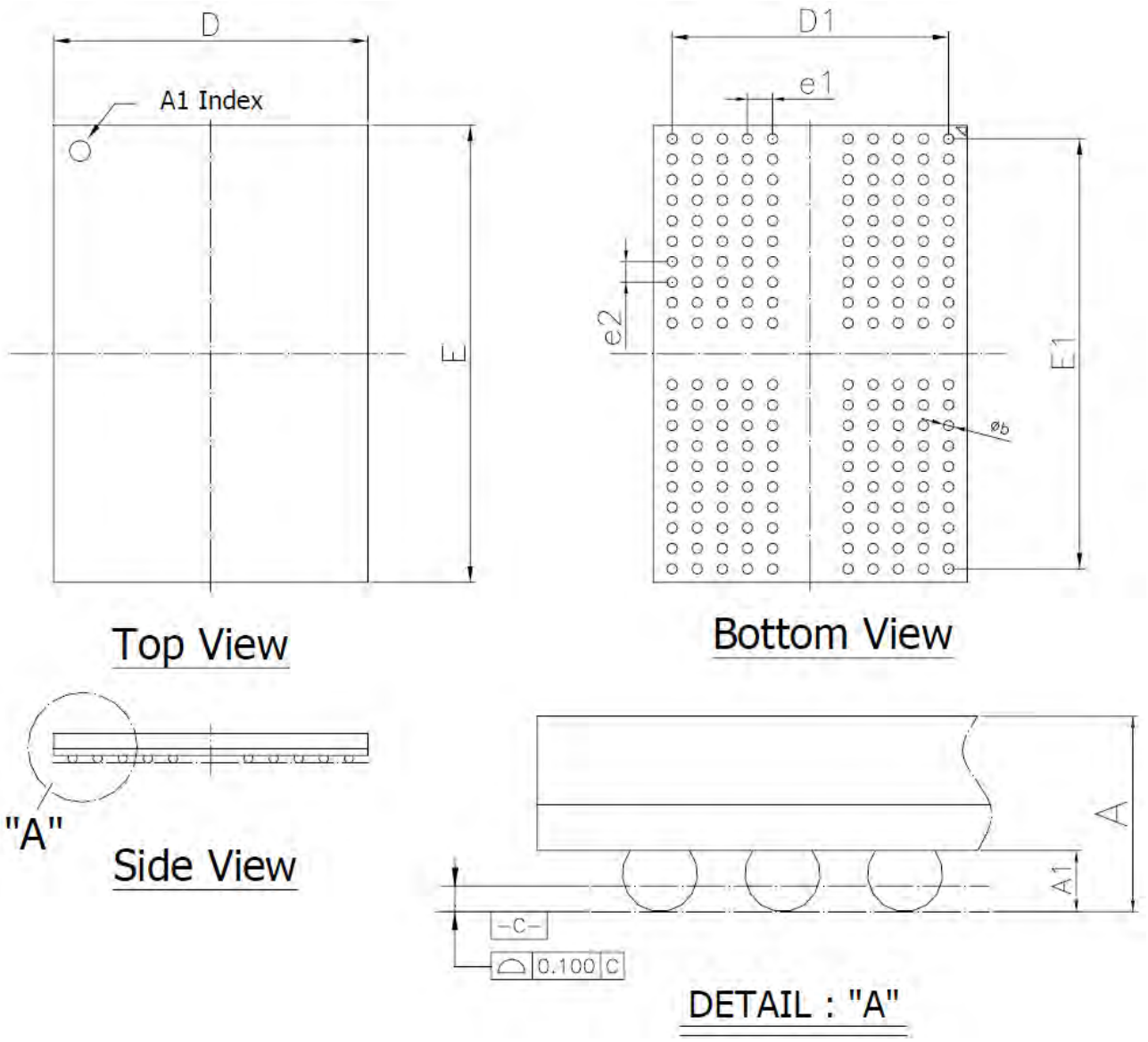
t_{CKCKEH}	Valid Clock Requirement before CKE input High	max(1.75ns, 3nCK)	-	max(1.75ns, 3nCK)	-	-
t_{MRZ}	CA Bus Training CKE High to DQ Tri-state	1.5	-	1.5	-	ns
$t_{CKELODTon}$	ODT turn-on Latency from CKE	20	-	20	-	ns
$t_{CKELODToff}$	ODT tum-off Latency from CKE	20	-	20	-	ns
t_{XCBT_Short}	Exit Command Bus Training Mode to next valid command delay[42]	max(5nCK, 200ns)	-	max(5nCK, 200ns)	-	-
t_{XCBT_Middle}						-
t_{XCBT_Long}						-
Temperature Derating[43]						
t_{DQSCK}	DQS output access time from CK/CK# (derated)	3600	-	3600	-	ps
t_{RCD}	RAS-to-CAS delay (derated)	t_{RCD} + 1.875	-	t_{RCD} + 1.875	-	ns
t_{RC}	Activate-to- Activate command period (derated)	t_{RC} + 3.75	-	t_{RC} + 3.75	-	ns
t_{RAS}	Row active time (derated)	t_{RAS} +1.875	-	t_{RAS} +1.875	-	ns
t_{RP}	Row precharge time (derated)	t_{RP}+ 1.875	-	t_{RP}+ 1.875	-	ns
t_{RRD}	Active bank A to active bank B (derated)	t_{RRD} + 1.875	-	t_{RRD} + 1.875	-	ns

Notes:

1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
2. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.
3. The deterministic component of the total timing. Measurement method tbd.
4. This parameter will be characterized and guaranteed by design.
5. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
6. tQSL describes the instantaneous differential output low pulse width on DQS – DQS#, as it measured the next rising edge from an arbitrary falling edge.
7. tQSH describes the instantaneous differential output high pulse width on DQS – DQS#, as it measured the next rising edge from an arbitrary falling edge.
8. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
9. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies> 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
10. tDQSCK_temp max delay variation as a function of Temperature.
11. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1- tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement VDDQ = VDD2 is assumed.
12. The same voltage and temperature are applied to tDQS2CK_rank2rank.
13. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
14. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
15. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
16. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
17. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
18. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
19. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
20. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
21. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
22. TDQS2DQ max delay variation as a function of temperature.
23. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ = VDD2 is assumed.
24. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
25. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
26. VIHL_AC does not have to be met when no transitions are occurring.
27. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
28. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
29. The length of Write Postamble depends on MR3 OP1 setting.
30. Delay time has to satisfy both analog time(ns) and clock count(nCK).
31. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
32. Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).

33. Vcent_CA must be within the adjustment range of the CA internal Vref.
34. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
35. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
36. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
37. VIHL_AC does not have to be met when no transitions are occurring.
38. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 x tCK) and 1.75ns has transpired.
39. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.
40. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
41. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
42. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Package Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.0315	--	--	0.80
A1	0.0067	--	0.0110	0.17	--	0.28
D	0.3898	0.3937	0.3976	9.90	10.00	10.10
E	0.5669	0.5709	0.5748	14.40	14.50	14.60
D1	--	0.3465	--	--	8.80	--
E1	--	0.5374	--	--	13.65	--
e1	--	0.0315	--	--	0.80	--
e2	--	0.0256	--	--	0.65	--
b	0.0106	0.0126	0.0146	0.27	0.32	0.37

Figure 22. 200-Ball FBGA Package 10x14.5x0.8mm (max)

PART NUMBERING SYSTEM

LPDDR4X PART NUMBERING SYSTEM									
AS4C	**MHyMOH**	**MD4V**	**A**	**-**	**62**	**B**	**C/I/A**	**N**	**XX**
AS : Alliance Memory 4C : DRAM Product Line	**Memory Organization** **MHyMOH:** 4Gb (MHyMxOH)	**Product MD4V :** LPDDR4X	**Blank** : initial release **A** : Die Rev.A	-	**Max Clock** **062:** 1600MHz **053:** 1866MHz **046:** 2133MHz	**Package** **B:**FBGA	**Temperature** **C:**Commercial **I :** Industrial **A:**Automotive	**N**: Lead Free &Halogen Free	**Packing Media** **None:** Tray **TR :** Reel

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