Reliability Qualification Report
for
AS25F364MQ-10WIN

64Mb (x1/x2/x4) 3.3V Serial Multi I/O NOR Flash Memory
PACKAGE TYPE : 8L WSON (6x5mm)

Issued Date: September 23, 2021

RELIABILITY TEST DATA

1. Long-Term Dynamic Life Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.		
				168H	500H	1000H
Ta=125°C Vdd=3.6V Fmax=1MHz Time=1000Hrs	JESD22 A108	AALA028000	77	0	0	0

2. Temperature Humidity Bias Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.		
				168H	500H	1000H
Ta=85°C 85% R.H. Vdd=3.6V Time=1000Hrs	EIAJ-ED-4701 B-122	AALA028000	77	0	0	0

3. High Temperature Storage Life Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.		
				168H	500H	1000H
Temp=150°C Time=1000Hrs	JESD22 A103-A	AALA028000	77	0	0	0

4. Failure Unit Calculation :

Test Items	Test Hours	Test Sample	Failure No.	FIT at 55°C	MTTF at 55°C (Hours)
Long-Term Dynamic Life Test	1000H	77	0	154	6.49E+06

Note :

1. Ta=125°C , Ea=0.7eV , β=1 , Confidence Level=60%
2. FIT : Failure Unit , 1 FIT is One Failure in 1.0E+09 Device-Hours
3. Failure Unit Calculation :

$$\lambda(T)=\frac{X^2(2n+2,1-CL)}{2*N*t}$$

$\lambda(T)$=Failure Rate

X^2=Chi-Square Function

n=Failure No.

CL=Confidence Level

Where

N=Test Sample
t= Test Time
T= Test Temperature in °K

$$AF(V)=F(V_1,V_2)=Exp[\beta(V_1 - V_2)]$$

AF(V)=Voltage Acceleration Factor
V_1=Test Voltage
V_2=Desired Voltage
β=Voltage Acceleration Constant

$$AF(T)=F(T_1,T_2)=Exp[-\frac{E_a}{K}(\frac{1}{T_1}-\frac{1}{T_2})]$$

AF(T)=Temperature Acceleration Factor
Ea=Activation Energy
K=Boltzman's Constant ($8.63*10^{-5}$ eV / °K)
T_1=Test Temperature in °K
T_2=Desired Temperature in °K

$$AF = F(V_1, V_2) * F(T_1 , T_2)$$

$$FIT = \frac{\lambda(T)}{AF}$$

$$MTTF = \frac{1}{FIT}$$

5. Electrostatic Discharge (ESD) Testing :

5-1. Human Body Model (Ref. Spec : MIL-STD-883E Method 3015.7) :ESD CLASSIFICATION-2

Test Condition	Test Mode	Lot no.	Sample Size	Pass ESD Sensitivity Pang in Voltages / Sample Size
R=1.5KΩ C=100pF	I/P-VSS	AALA028000	3	> ±2000V / 3
	I/P-VDD		3	> ±2000V / 3
	I/P-I/O		3	> ±2000V / 3
	I/O-VSS		3	> ±2000V / 3
	I/O-VDD		3	> ±2000V / 3
	VDD-VSS		3	> ±2000V / 3

5-2. Machine Model (Ref. Spec : EIAJ ED-4701 Method C-111) : ESD CLASSIFICATION-M2

Test Condition	Test Mode	Lot no.	Sample Size	Pass ESD Sensitivity Pang in Voltages / Sample Size
R=0Ω C=200pF	I/P-VSS	AALA028000	3	> ±200V / 3
	I/P-VDD		3	> ±200V / 3
	I/P-I/O		3	> ±200V / 3
	I/O-VSS		3	> ±200V / 3
	I/O-VDD		3	> ±200V / 3
	VDD-VSS		3	> ±200V / 3

5-3. CDM Model (Ref. Spec : JESD22-C101) : ESD CLASSIFICATION-III

Test Condition	Lot no.	Test Voltage	Sample Size	Test Result
Non-Socket Type Field Charge	AALA028000	+200V	3	Pass
		-200V	3	Pass
		+500V	3	Pass
		-500V	3	Pass

6. Latch-Up Test (Ref. Spec. : JEDEC Standard No.78) :

Trigger Mode	Test Pin	Lot no.	Sample Size	Triggering Source Induce Latch-Up / Sample Size
+IT	I/P	AALA028000	3	+200mA / 3
	I/O			+200mA / 3
-IT	I/P		3	-200mA / 3
	I/O			-200mA / 3
Vsupply Over Voltage Test	Vcc		3	± 1.5xVcc(max.) / 3

7. Preconditioning Stress Sequence :

Test Flow	Ref. Spec.	Lot No.	Test Conditions
Bake	IPC/JEDEC J-STD-020E	AALA028000	24Hrs , 125°C
T/H Soaking			Level III , 30°C / 60% R.H., 192Hrs
IR Reflow			3 Times , 265°C Max.

8. Temperature Cycling Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.	
				500°C	1000°C
-65°C ↔ 150°C 10min 10min 1000Cycles	MIL-STD-883E 1010.7	AALA028000	45*	0	0

9. Thermal Shock Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.	
				500°C	1000°C
-65°C ↔ 150°C 5min 5min 1000Cycles	MIL-STD-883E 1011.9	AALA028000	45*	0	0

10. Pressure Cooker Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.
				168H
121°C,15PSIG 100% R.H. 168HRS	JEDEC STD No. A102-1 22-B	AALA028000	45*	0

* : With Preconditioning Performed.

11. Solderability Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No. (<95% Coverage)
245±5°C, 5Secs With Steam 8Hrs	MIL-STD-883E 2003.7	AALA028000	15	0

12. Resistance to Soldering Heat Test :

Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.
260±5°C 10±0.5s	EIAJ-ED4701 A-132	AALA028000	15	0

13. Manual Soldering Test :

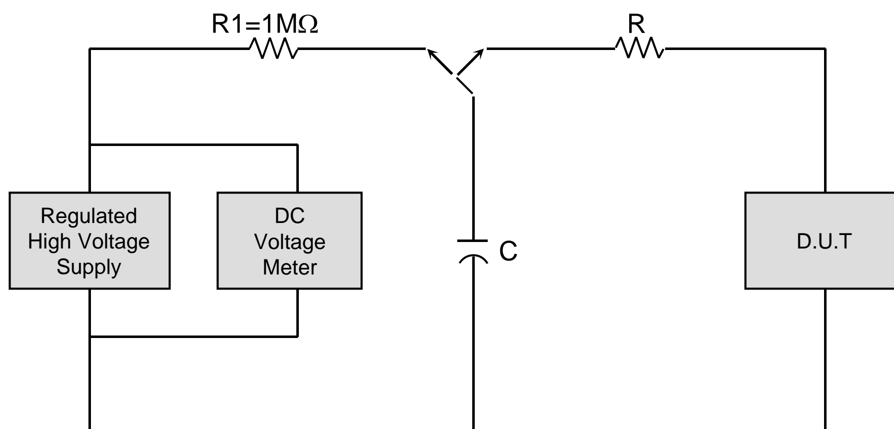
Test Conditions	Ref. Spec.	Lot No.	Sample Size	Failure No.
380°C 3Secs	-	AALA028000	5	0

ELECTROSTATIC DISCHARGE (ESD) TESTING

1. Purpose :

The purpose of this test is to measure the electrostatic discharge sensitivity caused by handling the microelectronic device.

2. Testing Configuration :



Reference Standard	R	C
MIL-STD-883E Method 3015.7	1.5 KΩ	100 pF
EIAJ ED-4701 Method C-111	0 KΩ	200 pF

3. Pin Combinations :

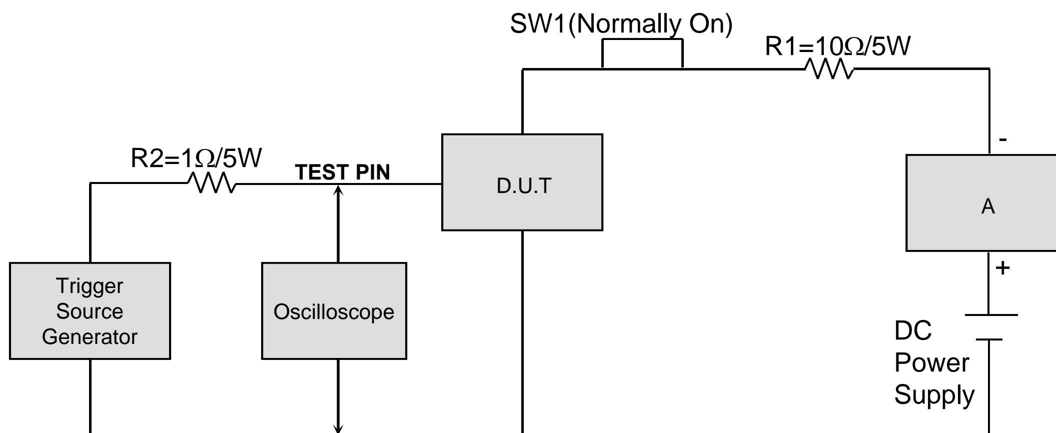
I/P – VSS	I/O – VSS	O/P – VSS
I/P – VDD	I/O – VDD	O/P – VDD
I/P – I/O	I/O – O/P	VDD – VSS
I/P – O/P		

LATCH-UP TESTING

1. Purpose :

The purpose of this test is to measure the Latch-Up Susceptibility of CMOS device induced by triggering source.

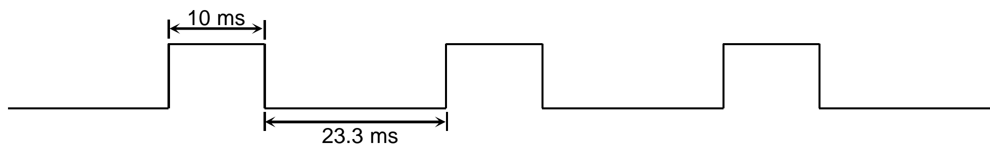
2. Testing Configuration :



The triggering source is applied as follows :

A. DC Current (IT)

B. Voltage Pulse (VT)



3. Test procedure for Latch-Up test :

A. Apply the triggering source to the test pin.

B. Measure the device supply current and record the triggering voltage or triggering current if Latch-Up occurs.

C. Increase the triggering source if Latch-Up does not occur.

D. Repeat steps A , B and until Latch-Up occur.