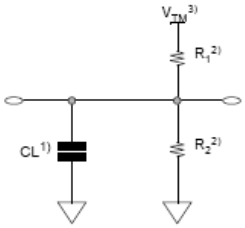
AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)
Input Pulse Level : 0.4 to 2.4V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : $CL^{1)}$ = 100pF+ 1 TTL(70nsec)
$CL^{1)}$ = 30pF + 1 TTL(45ns/55ns)
1. Including scope and Jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM}=2.8V
4. CL = 5pF + 1 TTL (measurement with t_{LZ}, t_{HZ}, t_{OLZ}, t_{OHZ}, t_{WHZ})



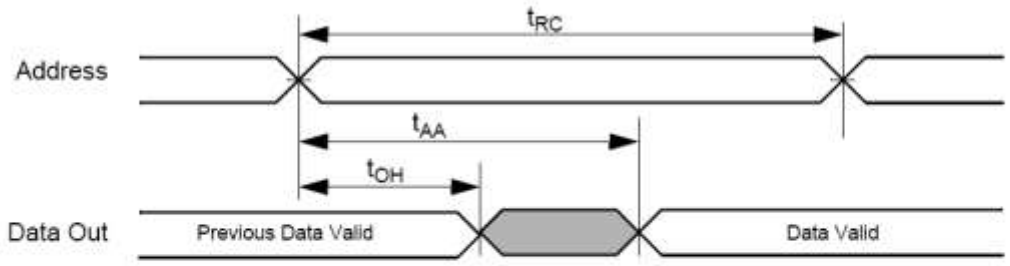
READ CYCLE (V_{CC} =2.7 to 3.6V, Gnd = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	45ns		Unit
		Min	Max	
Read cycle time	^tRC	45	-	ns
Address access time	^tAA	-	45	ns
Chip select to output	$^tCO1$, $^tCO2$	-	45	ns
Output enable to valid output	^tOE	-	30	ns
Chip select to low-Z output	$^tLZ1$, $^tLZ2$	5	-	ns
Output enable to low-Z output	^tOLZ	5	-	ns
Chip disable to high-Z output	$^tHZ1$, $^tHZ2$	0	20	ns
Output disable to high-Z output	^tOHZ	0	20	ns
Output hold from address change	^tOH	10	-	ns

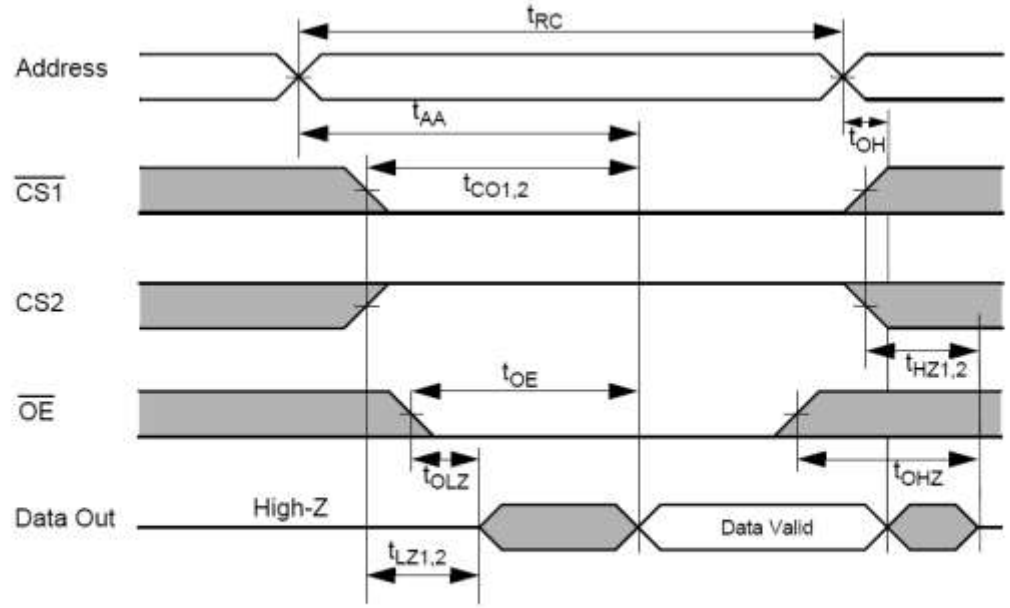
Parameter	Symbol	45ns		Unit
		Min	Max	
Write cycle time	^tWC	45	-	ns
Chip select to end of write	$^tCW1$,$^tCW2$	45	-	ns
Address setup time	^tAS	0	-	ns
Address valid to end of write	^tAW	45	-	ns
Write pulse width	^tWP	45	-	ns
Write recovery time	^tWR	0	-	ns
Write to ouput high-Z	^tWHZ	0	20	ns
Data to write time overlap	^tDW	25	-	ns
Data hold from write time	^tDH	0	-	ns
End write to output low-Z	^tOW	5	-	ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH})



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})

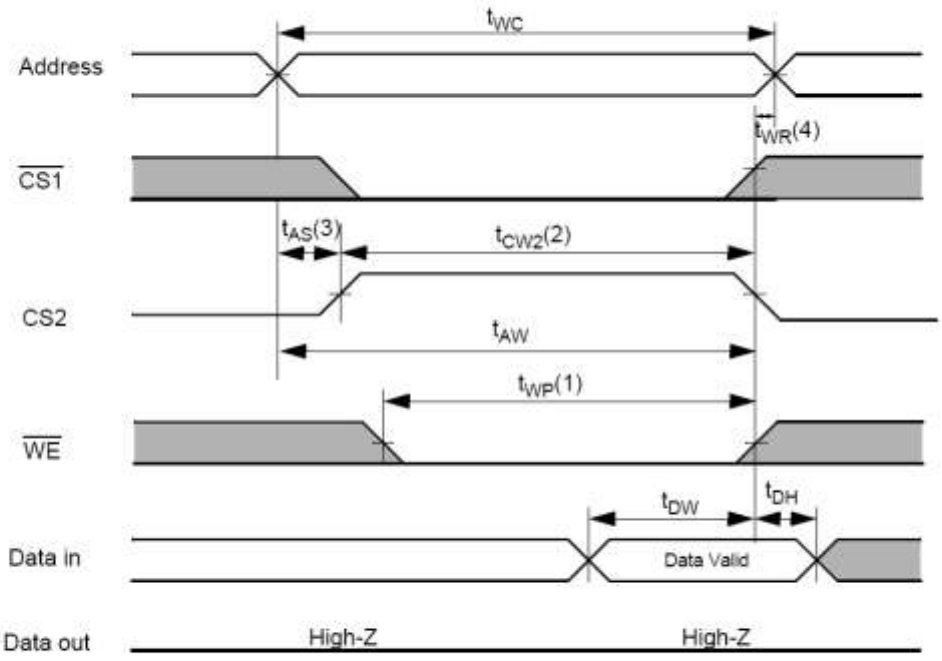


NOTES (READ CYCLE)

1.$t_{HZ1,2}$ and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2.At any given temperature and voltage condition, $t_{HZ1,2}$(Max.) is less than $t_{LZ1,2}$(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$, a high CS2 and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ goes low, CS2 goes high and $\overline{WE}$ goes low. A write ends at the earliest transition among $\overline{CS1}$ goes high, CS2 goes low and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low or CS2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low.

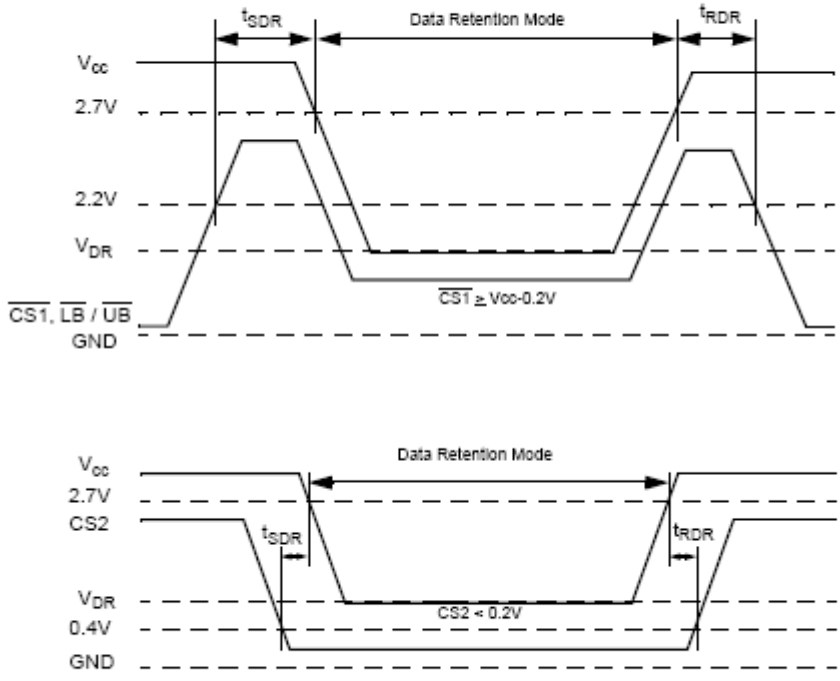
DATA RETENTION CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{CC} for Data Retention	^{v}DR	I_{SB1} Test Condition (Chip Disabled)[1)]	1.5	-	3.6	V
Data Retention Current	^{I}DR	V_{CC}=1.5V, I_{SB1} Test Condition (Chip Disabled)[1)]	-	-	4	µA
Chip Deselect to Data Retention Time	^{t}SDR	See data retention wave form	0	-	-	ns
Operation Recovery Time	^{t}RDR		^{t}RC	-	-	

NOTES

1. See the I_{SB1} measurement condition of datasheet page 5.

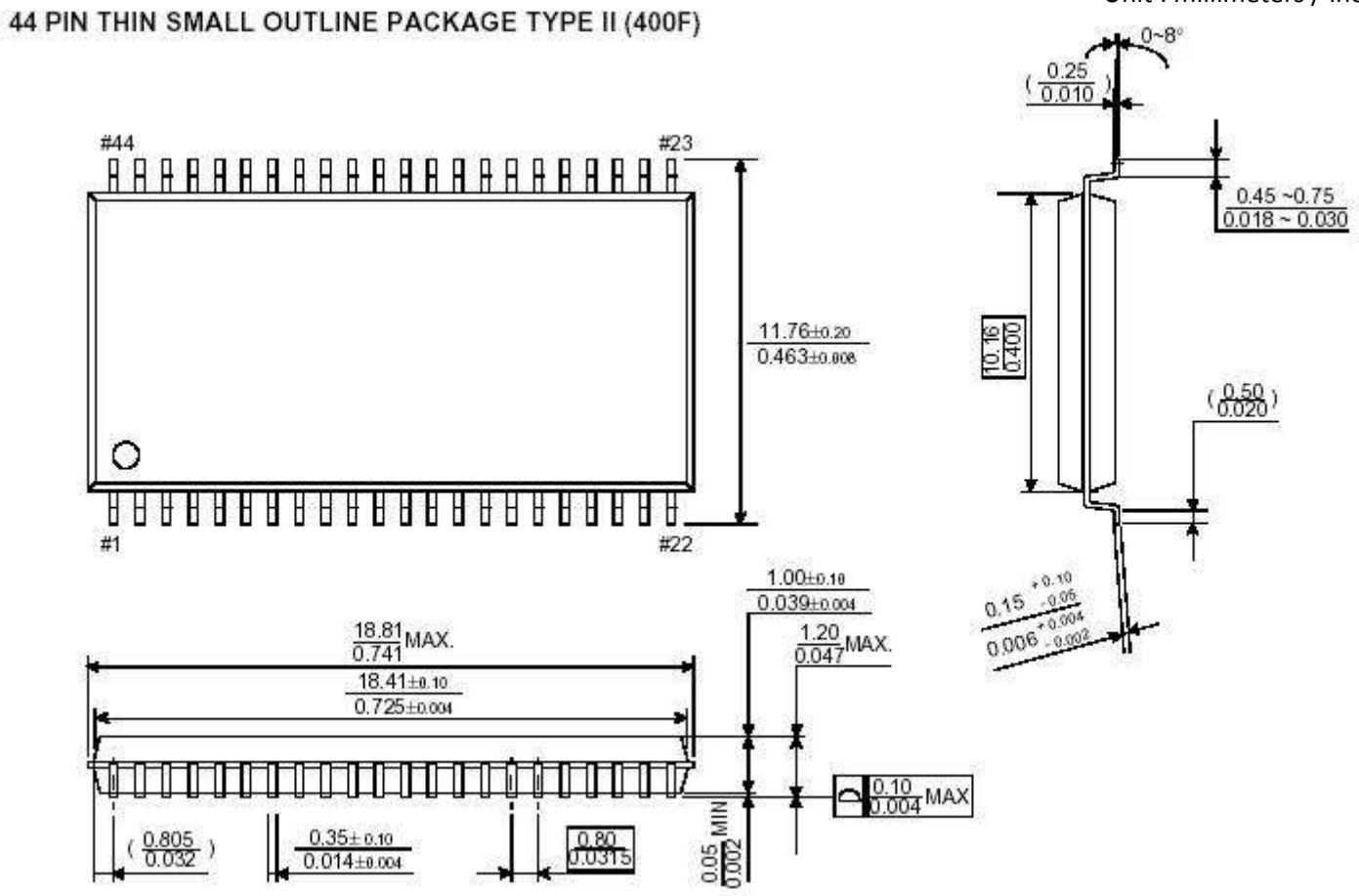
DATA RETENTION WAVE FORM



PACKAGE DIMENSION

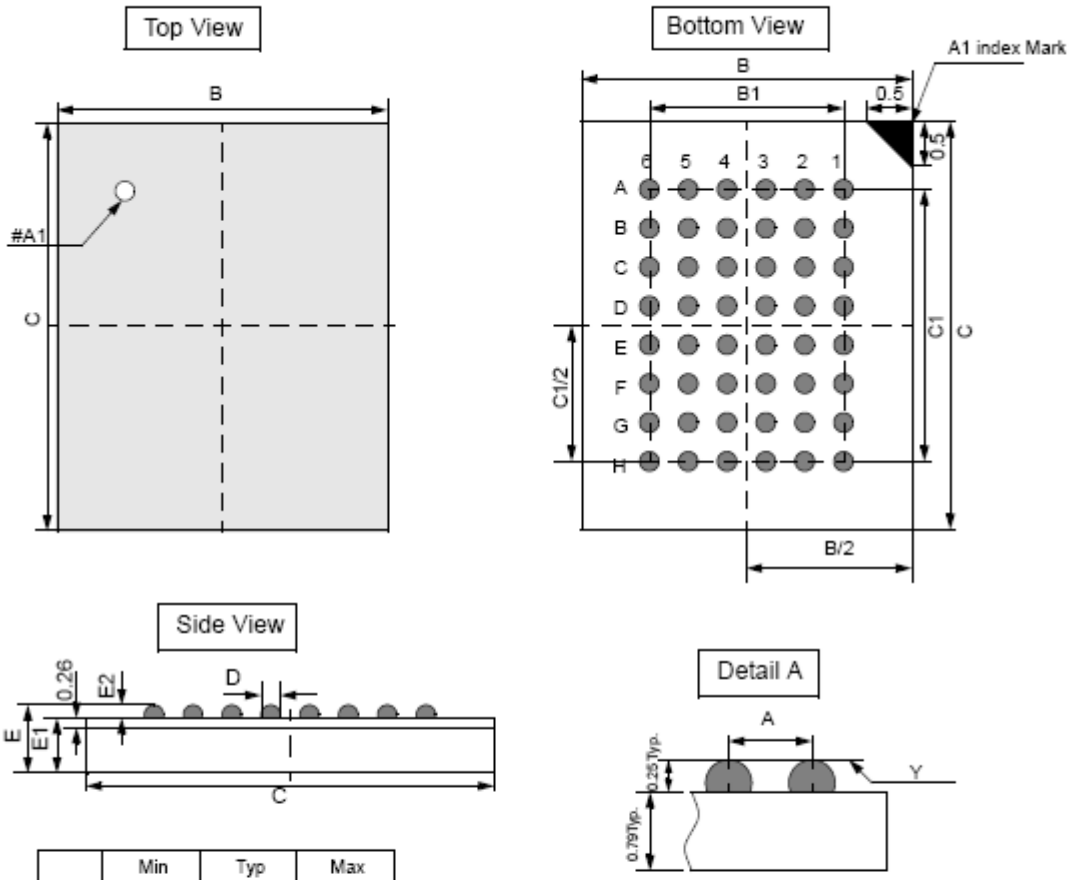
44 - TSOP2 (0.8mm pin pitch)

Unit : millimeters / inches



48 Ball Fine Pitch BGA (0.75mm ball pitch)

Unit: millimeters



	Min	Typ	Max
A	-	0.75	-
B	7.95	8.00	8.05
B1	-	3.75	-
C	9.95	10.00	10.05
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	-	1.00
E1	-	-	0.70
E2	0.20	0.25	0.30
Y	-	-	0.08

NOTES

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity : 0.08(Max)