



Comparison Between CY62256VNLL-70 and AS6C62256-55 256Kb LP-SRAM

Part number	CY62256VNLL-70SNXI CY62256VNLL-70SNXIT CY62256VNLL-70ZXC CY62256VNLL-70ZXCT CY62256VNLL-70ZXI CY62256VNLL-70ZXIT	AS6C62256-55SIN AS6C62256-55SINTR AS6C62256-55STCN AS6C62256-55STCNTR AS6C62256-55STIN AS6C62256-55STINTR	Comparison result
Power supply	2.7V – 3.6V	2.7V – 5.5V	Alliance Memory offers a wider voltage range, which covers the range for the Cypress parts
Typical power dissipation under normal operation	Speed: 70ns Average operating power supply current I _{cc} = 30mA (max.) I _{cc} = 11mA (typ.) Standby power (μA) Supply current -TTL inputs ISB1 = 300μA (max.) ISB1 = 100μA (typ.) -CMOS inputs ISB2 = 10μA (max., I temp.) ISB2 = 0.1μA (typ. I temp)	Speed: 55ns Average operating power supply current I _{cc} = 45mA (max.) I _{cc} = 15mA (typ.) I _{cc1} = 10mA (max.) I _{cc1} = 3mA (typ.) Standby power (μA) Supply current -TTL inputs ISB = 3mA (max.) ISB = 1mA (typ.) ISB1 = 30μA (max., I temp.) ISB1 = 15μA (max., C temp.) ISB1 = 1μA (typ., C/I temp.)	The AS6C62256-55's faster speed covers the Cypress parts, and there is a supply current different
Operating temperature	Industrial: -40°C to +85°C Commercial: 0°C to +70°C	Industrial: -40°C to +85°C Commercial: 0°C to +70°C	Same
Max. operating speed	70ns	55ns	Same
Interface (input/output) capacitance	Input capacitance C _{IN} : <6pF Output capacitance C _O : <8pF	Input capacitance C _{IN} : <6pF Output capacitance C _O : <8pF	Same
Interface definition	Omit (see datasheet)	Omit (see datasheet)	Same. They are pin-to-pin compatible
Timing parameters	Refer to "Annex 1"	Refer to "Annex 1"	Compatible
Timing diagram and command	Omit (see datasheet)	Omit (see datasheet)	Same
Capacity	256Kb	256Kb	Same
Package	28-pin, 300-mil SOP 28-pin TSOP (8 mm x 13.4 mm)	28-pin, 330-mil SOP 28-pin TSOP (8 mm x 13.4 mm)	They are pin-to-pin compatible. The package size is the same. Alliance Memory and Cypress use

			different package code names
Truth table	Omit (see datasheet)	Omit (see datasheet)	Same

Annex 1: Comparison Between the AC Electrical Characteristics of the CY62256VNLL-70 and AS6C62256-55

Read Cycle						
Parameter	Symbol	CY62256VNLL-70		AS6C62256-55		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	tRC	70	-	55	-	ns
Address access time	tAA	-	70	-	55	ns
Chip enable access time	tACE	-	70	-	55	ns
Output enable access time	tOE	-	35	-	30	ns
Chip enable to output in low-Z	tCLZ*	10	-	10	-	ns
Output enable to output in low-Z	tOLZ*	5	-	5	-	ns
Chip disable to output in high-Z	tCHZ*	-	25	-	20	ns
Output disable to output in high-Z	tOHZ*	-	25	-	20	ns
Output hold from address change	tOH	10	-	10	-	ns
Write Cycle						
Parameter	Symbol	CY62256VNLL-70		AS6C62256-55		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tWC	70	-	55	-	ns
Address valid to end of write	tAW	60	-	50	-	ns
Chip enable to end of write	tCW	60	-	50	-	ns
Address set-up time	tAS	0	-	0	-	ns
Write pulse width	tWP	50	-	45	-	ns
Write recovery time	tWR	0	-	0	-	ns
Data to write time overlap	tDW	30	-	25	-	ns
Data hold from end of write time	tDH	0	-	0	-	ns
Output active from end of write	tOW*	10	-	5	-	ns
Write to output in high-Z	tWHZ*	-	25	-	20	ns