Revision History
256Mb AS4C16M16D1-5BAN 96 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Initial Release	Aug.2020

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Features

- Fast clock rate: 200MHz
- AEC-Q100 Compliant
- Differential Clock CK & $\overline{CK}$
- Bi-directional DQS
- DLL enable/disable by EMRS
- Fully synchronous operation
- Internal pipeline architecture
- Four internal banks, 4M x 16-bit for each bank
- Programmable Mode and Extended Mode registers
  - CAS Latency: 2, 2.5, 3
  - Burst length: 2, 4, 8
  - Burst Type: Sequential & Interleaved
- Individual byte write mask control
- DM Write Latency = 0
- Auto Refresh and Self Refresh
  - Not support self refresh function with T_A > 85°C
- 8192 refresh cycles / 16ms
- Precharge & active power down
- Operating temperature: T_A = -40~105°C (Automotive)
- Power supplies: V_{DD} & V_{DDQ} = 2.5V ± 0.2V
- Interface: SSTL_2 I/O Interface
- Package: Pb free and Halogen free
  - 60 Ball, 8x13x1.2 mm (max) FBGA

Overview

The AS4C16M16D1 SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 256 Mbits. It is internally configured as a quad 4M x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK). Data outputs occur at both rising edges of CK and $\overline{CK}$.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a BankActivate command which is then followed by a Read or Write command. The AS4C16M16D1 provides programmable Read or Write burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The refresh functions, either Auto or Self Refresh are easy to use. In addition, AS4C16M16D1 features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance. These devices are well suited for applications requiring high memory bandwidth; result in a device particularly well suited to high performance main memory and graphics applications.

Table 1A. Ordering Information

Product part No	Org	Temperature	Max Clock (MHz)	Package
AS4C16M16D1-5BAN	16M x 16	Automotive -40°C to 105°C	200	60-ball FBGA

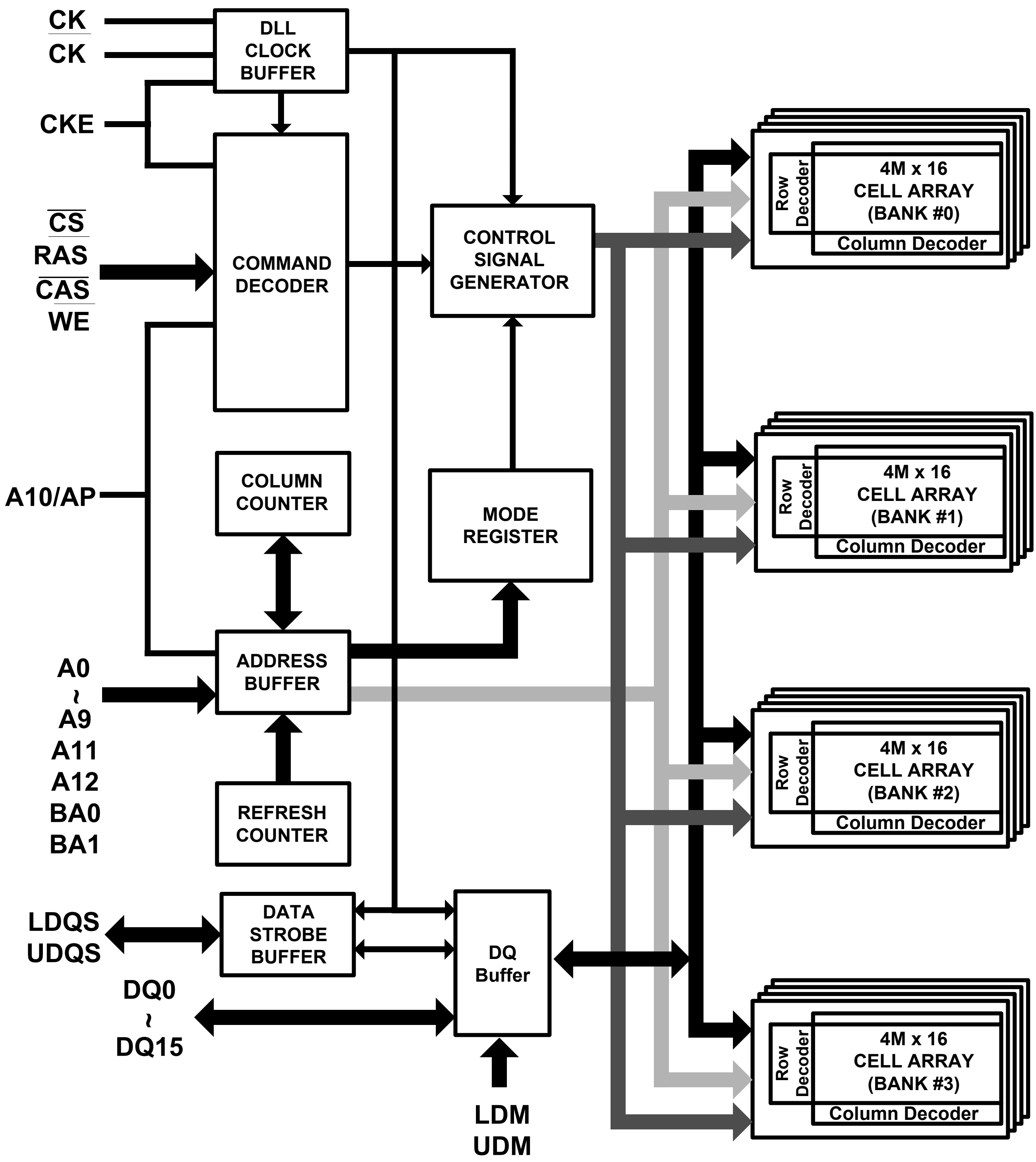
Table 1B. Speed Grade Information

Speed Grade	Clock Frequency	CAS Latency	tRCD(ns)	tRP(ns)
DDR1-400	200MHz	3	15	15

Figure 1. Ball Assignment (Top View)

	1	2	3	…	7	8	9
A	VSSQ	DQ15	VSS		VDD	DQ0	VDDQ
B	DQ14	VDDQ	DQ13		DQ2	VSSQ	DQ1
C	DQ12	VSSQ	DQ11		DQ4	VDDQ	DQ3
D	DQ10	VDDQ	DQ9		DQ6	VSSQ	DQ5
E	DQ8	VSSQ	UDQS		LDQS	VDDQ	DQ7
F	VREF	VSS	UDM		LDM	VDD	NC
G		CK	$\overline{CK}$		$\overline{WE}$	$\overline{CAS}$	
H		A12	CKE		$\overline{RAS}$	$\overline{CS}$	
J		A11	A9		BA1	BA0	
K		A8	A7		A0	A10	
L		A6	A5		A2	A1	
M		A4	VSS		VDD	A3	

Figure 2. Block Diagram



Pin Descriptions

Table 2. Pin Details

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Differential Clock:** CK, $\overline{CK}$ are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. Both CK and $\overline{CK}$ increment the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. If CKE goes low synchronously with clock, the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BA0, BA1	Input	**Bank Activate:** BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied.
A0-A12	Input	**Address Inputs:** A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/Write command (column address A0-A8 with A10 defining Auto Precharge).
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{RAS}$	Input	**Row Address Strobe:** The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH" either the Bank Activate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted "HIGH" the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW" the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
$\overline{CAS}$	Input	**Column Address Strobe:** The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ is held "HIGH" and $\overline{CS}$ is asserted "LOW" the column access is started by asserting $\overline{CAS}$ "LOW". Then, the Read or Write command is selected by asserting $\overline{WE}$ "HIGH" or "LOW".
$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command.
LDQS, UDQS	Input / Output	**Bidirectional Data Strobe:** Specifies timing for Input and Output data. Read Data Strobe is edge triggered. Write Data Strobe provides a setup and hold time for data and DQM. LDQS is for DQ0~7, UDQS is for DQ8~15.
LDM, UDM	Input	**Data Input Mask:** Input data is masked when DM is sampled HIGH during a write cycle. LDM masks DQ0-DQ7, UDM masks DQ8-DQ15.
DQ0 - DQ15	Input / Output	**Data I/O:** The DQ0-DQ15 input and output data are synchronized with positive and negative edges of LDQS and UDQS. The I/Os are byte-maskable during Writes.
V_{DD}	Supply	**Power Supply:** 2.5V $\pm$ 0.2V .
V_{SS}	Supply	**Ground**

V_{DDQ}	Supply	**DQ Power:** 2.5V ± 0.2V. Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
V_{REF}	Supply	**Reference Voltage for Inputs:** +0.5 x V_{DDQ}.
NC	-	**No Connect:** These pins should be left unconnected.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 3 shows the truth table for the operation commands.

Table 3. Truth Table (Note (1), (2))

Command	State	CKE$_{n-1}$	CKE$_n$	DM	BA0,1	A10	A0-9, 11-12	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
BankActivate	Idle(3)	H	X	X	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	Column address (A0 ~ A8)	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	X	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	L	Column address (A0 ~ A8)	L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	H		L	H	L	H
(Extended) Mode Register Set	Idle	H	X	X	OP code			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active(4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AutoRefresh	Idle	H	H	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (SelfRefresh)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Precharge Power Down Mode Entry	Idle	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Precharge Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Active Power Down Mode Entry	Active	H	L	X	X	X	X	H	X	X	X
								L	V	V	V
Active Power Down Mode Exit	Any (PowerDown)	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Input Mask Disable	Active	H	X	L	X	X	X	X	X	X	X
Data Input Mask Enable(5)	Active	H	X	H	X	X	X	X	X	X	X

Note:

1. V=Valid data, X=Don't Care, L=Low level, H=High level.
2. CKE$_n$ signal is input level when commands are provided.
   CKE$_{n-1}$ signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA signal.
4. Device state is 2, 4, and 8 burst operation.
5. LDM and UDM can be enabled respectively.

Mode Register Set (MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs CAS Latency, Burst Type, and Burst Length to make the DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed. The Mode Register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A12 and BA0, BA1 in the same cycle in which $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are asserted Low is written into the Mode Register. A minimum of two clock cycles, tMRD, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and CAS Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and CAS latencies.

Table 4. Mode Register Bitmap

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	0	RFU must be set to “0”				T.M.		CAS Latency			BT	Burst Length			Mode Register

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset
X	1	Test mode

BA0	Mode
0	MRS
1	EMRS

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

- Burst Length Field (A2~A0)

  This field specifies the data length of column access using the A2~A0 pins and selects the Burst Length to be 2, 4, 8.

Table 5. Burst Length

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

- Addressing Mode Select Field (A3)

  The Addressing Mode can be one of two modes, either Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4 and 8.

Table 6. Addressing Mode

A3	Addressing Mode
0	Sequential
1	Interleave

- Burst Definition, Addressing Sequence of Sequential and Interleave Mode

Table 7. Burst Address ordering

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

- CAS Latency Field (A6~A4)

  This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field. $t_{CAC}(min) \leq$ CAS Latency X t_{CK}

Table 8. CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2 clocks
0	1	1	3 clocks
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5 clocks
1	1	1	Reserved

- Test Mode field (A8~A7)

  These two bits are used to enter the test mode and must be programmed to "00" in normal operation.

Table 9. Test Mode

A8	A7	Test Mode
0	0	Normal mode
1	0	DLL Reset

- (BA0, BA1)

Table 10. MRS/EMRS

BA1	BA0	A12 ~ A0
RFU	0	MRS Cycle
RFU	1	Extended Functions (EMRS)

Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. The state of A0 ~ A12, BA0 and BA1 is written in the mode register in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ going low. (The device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be high). A1 is used for setting driver strength to normal, or weak. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

Table 11. Extended Mode Register Bitmap

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
0	1	RFU must be set to “0”						DS1	RFU must be set to “0”				DS0	DLL	Extended Mode Register

BA0	Mode
0	MRS
1	EMRS

A6	A1	Drive Strength	Comment
0	0	Full	
0	1	Weak	
1	0	RFU	Reserved For Future
1	1	Matched impedance	Output driver matches impedance

A0	DLL
0	Enable
1	Disable

Table 12. Absolute Maximum Rating

Symbol	Item	Values	Unit
$V_{I/O}$	Voltage on I/O Pins Relative to Vss	-0.5 ~ V_{DDQ} + 0.5	V
V_{DD}, V_{DDQ}	Voltage on V_{DD}, V_{DDQ} Supply Relative to Vss	-1 ~ 3.6	V
V_{IN}	Voltage on Inputs Relative to Vss	-1 ~ 3.6	V
T_A	Ambient Temperature	-40 ~ 105	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Output Current	50	mA

Note: Absolute maximum DC requirements contain stress ratings only. Functional operation at the absolute maximum limits is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability.

Table 13. Recommended D.C. Operating Conditions (V_{DD} = 2.5V ±0.2V, T_A = -40~105 °C)

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Power Supply Voltage	2.3	2.7	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	2.3	2.7	V
V_{REF}	Input Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V
V_{IH} (DC)	Input High Voltage (DC)	V_{REF} + 0.15	V_{DDQ} + 0.3	V
V_{IL} (DC)	Input Low Voltage (DC)	-0.3	V_{REF} - 0.15	V
V_{TT}	Termination Voltage	V_{REF} - 0.04	V_{REF} + 0.04	V
V_{IN} (DC)	Input Voltage Level, CK and $\overline{CK}$ inputs	-0.3	V_{DDQ} + 0.3	V
V_{ID} (DC)	Input Different Voltage, CK and $\overline{CK}$ inputs	0.36	V_{DDQ} + 0.6	V
I_I	Input leakage current	-2	2	µA
I_{OZ}	Output leakage current	-5	5	µA
I_{OH}	Output High Current (V_{OH} = 1.95V)	-16.2	-	mA
I_{OL}	Output Low Current (V_{OL} = 0.35V)	16.2	-	mA

Note: All voltages are referenced to V_{SS}.

Table 14. Capacitance (V_{DD} = 2.5V, T_A = 25 °C)

Symbol	Parameter	Min.	Max.	Delta	Unit
C_{IN1}	Input Capacitance (CK, $\overline{CK}$)	1.5	2.5	0.25	pF
C_{IN2}	Input Capacitance (All other input-only pins)	1.5	2.5	0.5	pF
$C_{I/O}$	DQ, DQS, DM Input/Output Capacitance	3.5	4.5	0.5	pF

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested

Table 15. D.C. Characteristics (V_{DD} = 2.5V ± 0.2V, T_A = -40~105 °C)

Parameter & Test Condition	Symbol	-5 Max.	Unit	Note
OPERATING CURRENT: One bank; Active-Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	78	mA	
OPERATING CURRENT: One bank; Active-Read-Precharge; BL=4; tRC=tRC(min); tCK=tCK(min); Iout=0mA; Address and control inputs changing once per clock cycle	IDD1	84	mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; tCK=tCK(min); CKE=LOW	IDD2P	6	mA	
PRECHARGE FLOATING STANDBY CURRENT: CKE = HIGH; $\overline{CS}$ =HIGH(DESELECT); All banks idle; tCK=tCK(min); Address and control inputs changing once per clock cycle; VIN=VREF for DQ, DQS and DM	IDD2F	36	mA	
PRECHARGE QUIET STANDBY CURRENT: CKE = HIGH; $\overline{CS}$ =HIGH(DESELECT); All banks idle; tCK=tCK(min); Address and other control input stadle at HIGH or LOW; VIN=VREF for DQ, DQS and DM	IDD2Q	24	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: one bank active; power-down mode; CKE=LOW; tCK=tCK(min)	IDD3P	24	mA	
ACTIVE STANDBY CURRENT: $\overline{CS}$ =HIGH;CKE=HIGH; one bank active ; tRC=tRC(max);tCK=tCK(min);Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	66	mA	
OPERATING CURRENT BURST READ: BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); Iout=0mA;50% of data changing on every transfer	IDD4R	120	mA	
OPERATING CURRENT BURST Write: BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; tCK=tCK(min); DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	120	mA	
AUTO REFRESH CURRENT: tRC=tRFC(min); tCK=tCK(min)	IDD5	120	mA	
SELF REFRESH CURRENT: Self Refresh Mode ; CKE≦ 0.2V; tCK=tCK(min)	IDD6	4	mA	1
BURST OPERATING CURRENT 4 bank operation: Four bank interleaving READs; BL=4;with Auto Precharge; tRC=tRC(min); tCK=tCK(min); Address and control inputs change only during Active, READ , or WRITE command	IDD7	168	mA	

Table 16. Electrical Characteristics and Recommended A.C.Operating Condition

(V_{DD} = 2.5V ±0.2V, T_A = -40~105 °C)

Symbol	Parameter		-5 Min.	-5 Max.	Unit	Note
t_{CK}	Clock cycle time	CL = 2	7.5	12	ns	
		CL = 2.5	6	12	ns	
		CL = 3	5	12	ns	
t_{CH}	Clock high level width		0.45	0.55	t_{CK}	
t_{CL}	Clock low level width		0.45	0.55	t_{CK}	
t_{HP}	Clock half period		$(t_{CL}, t_{CH})_{min}$	-	ns	2
t_{HZ}	Data-out-high impedance time from CK, $\overline{CK}$		-	0.7	ns	3
t_{LZ}	Data-out-low impedance time from CK, $\overline{CK}$		-0.7	0.7	ns	3
t_{DQSCK}	DQS-out access time from CK, $\overline{CK}$		-0.6	0.6	ns	
t_{AC}	Output access time from CK, $\overline{CK}$		-0.7	0.7	ns	
t_{DQSQ}	DQS-DQ Skew		-	0.4	ns	
t_{RPRE}	Read preamble		0.9	1.1	t_{CK}	
t_{RPST}	Read postamble		0.4	0.6	t_{CK}	
t_{DQSS}	CK to valid DQS-in		0.72	1.25	t_{CK}	
t_{WPRES}	DQS-in setup time		0	-	ns	4
t_{WPRE}	DQS write preamble		0.25	-	t_{CK}	
t_{WPST}	DQS write postamble		0.4	0.6	t_{CK}	5
t_{DQSH}	DQS in high level pulse width		0.35	-	t_{CK}	
t_{DQSL}	DQS in low level pulse width		0.35	-	t_{CK}	
t_{IS}	Address and Control input setup time		0.7	-	ns	6
t_{IH}	Address and Control input hold time		0.7	-	ns	6
t_{DS}	DQ & DM setup time to DQS		0.4	-	ns	
t_{DH}	DQ & DM hold time to DQS		0.4	-	ns	
t_{QH}	DQ/DQS output hold time from DQS		t_{HP} - t_{QHS}	-	ns	
t_{RC}	Row cycle time		55	-	ns	
t_{RFC}	Refresh row cycle time		70	-	ns	
t_{RAS}	Row active time		40	70k	ns	
t_{RCD}	Active to Read or Write delay		15	-	ns	
t_{RP}	Row precharge time		15	-	ns	
t_{RRD}	Row active to Row active delay		10	-	ns	
t_{WR}	Write recovery time		15	-	ns	
t_{WTR}	Internal Write to Read Command Delay		2	-	t_{CK}	
t_{MRD}	Mode register set cycle time		10	-	ns	
t_{REFI}	Average Periodic Refresh interval		-	1.95	μs	7
t_{XSRD}	Self refresh exit to read command delay		200	-	t_{CK}	
t_{XSNR}	Self refresh exit to non-read command delay		75	-	ns	
t_{DAL}	Auto Precharge write recovery + precharge time		t_{WR} + t_{RP}	-	ns	
t_{DIPW}	DQ and DM input puls width		1.75	-	ns	
t_{IPW}	Control and Address input pulse width		2.2	-	ns	
t_{QHS}	Data Hold Skew Factor		-	0.5	ns	
t_{DSS}	DQS falling edge to CK setup time		0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK		0.2	-	t_{CK}	
t_{RAP}	Active to Autoprecharge Delay		t_{RCD} or t_{RASmin}	-	ns	

Table 17. Recommended A.C. Operating Conditions (V_{DD} = 2.5V ±0.2V, T_A = -40~105 °C)

Symbol	Parameter	Min.	Max.	Unit
V_{IH} (AC)	Input High Voltage (AC)	V_{REF} + 0.31	-	V
V_{IL} (AC)	Input Low Voltage (AC)	-	V_{REF} - 0.31	V
V_{ID} (AC)	Input Different Voltage, CK and $\overline{CK}$ inputs	0.7	V_{DDQ} + 0.6	V
V_{IX} (AC)	Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	0.5 x V_{DDQ} - 0.2	0.5 x V_{DDQ} + 0.2	V

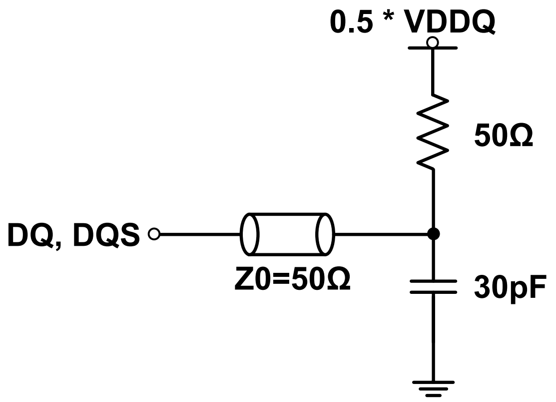
Note:

1) Enables on-chip refresh and address counters.
2) Min(t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and actual clock high time as provided to the device.
3) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ), or begins driving (LZ).
4) The specific requirement is that DQS be valid (High, Low, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic, and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
5) The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
6) For command/address slew rate ≧0.5V/ns and <1.0V/ns. For CK & $\overline{CK}$ slew rate ≧ 1.0V/ns.
7) A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
8) Power-up sequence is described in Note 10
9) A.C. Test Conditions

Table 18. SSTL _2 Interface

Reference Level of Output Signals (V_{REF})	0.5 x V_{DDQ}
Output Load	Reference to the Test Load
Input Signal Levels	V_{REF} + 0.31 V / V_{REF} - 0.31 V
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 x V_{DDQ}

Figure 3. SSTL_2 A.C. Test Load



10) **Power up Sequence**

Power up must be performed in the following sequence.

1. Apply power to V_{DD} before or at the same time as V_{DDQ}, V_{TT} and V_{REF} when all input signals are held "NOP" state and maintain CKE “LOW”.
2. Start clock and maintain stable condition for minimum 200μs.
3. Issue a “NOP” command and keep CKE “HIGH”
4. Issue a “Precharge All” command.
5. Issue EMRS – enable DLL.
6. Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
7. Precharge all banks of the device.
8. Issue two or more Auto Refresh commands.
9. Issue MRS – with A8 to low to initialize the mode register.

11) Overshoot/Undershoot Specification

Table 19. AC Overshoot/Undershoot Specification

Parameter	Values	Unit
Maximum peak amplitude allowed for overshoot	1.5	V
Maximum peak amplitude allowed for undershoot	1.5	V
The area between the overshoot signal and VDD must be less than or equal to	4.5	V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5	V-ns

Figure 4. Address and Control AC Overshoot and Undershoot Definition

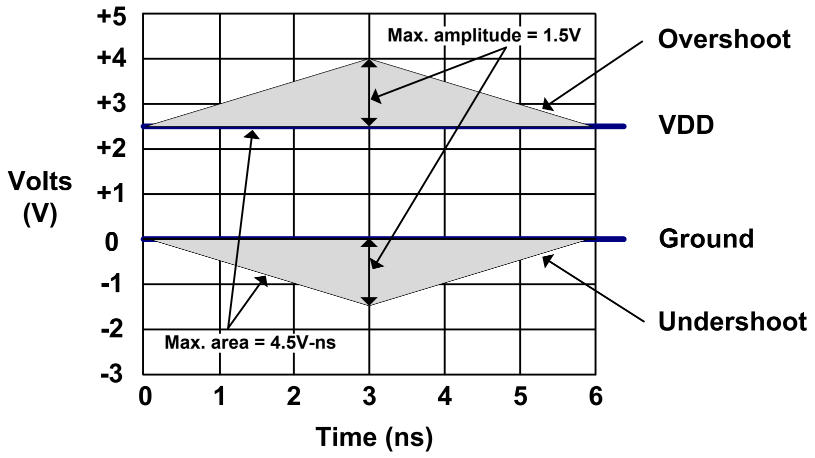
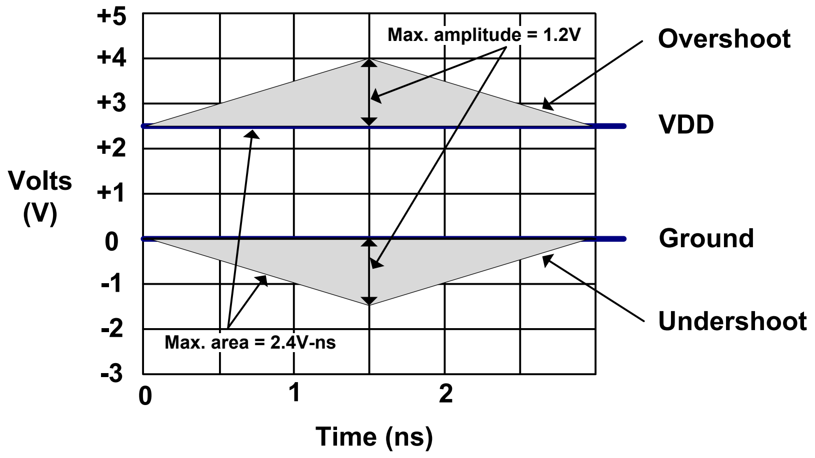


Table 20. AC Overshoot/Undershoot Specification

Parameter	Values	Unit
Maximum peak amplitude allowed for overshoot	1.2	V
Maximum peak amplitude allowed for undershoot	1.2	V
The area between the overshoot signal and VDD must be less than or equal to	2.4	V-ns
The area between the undershoot signal and GND must be less than or equal to	2.4	V-ns

Figure 5. DQ/DM/DQS AC Overshoot and Undershoot Definition



Timing Waveforms

Figure 6. Activating a Specific Row in a Specific Bank

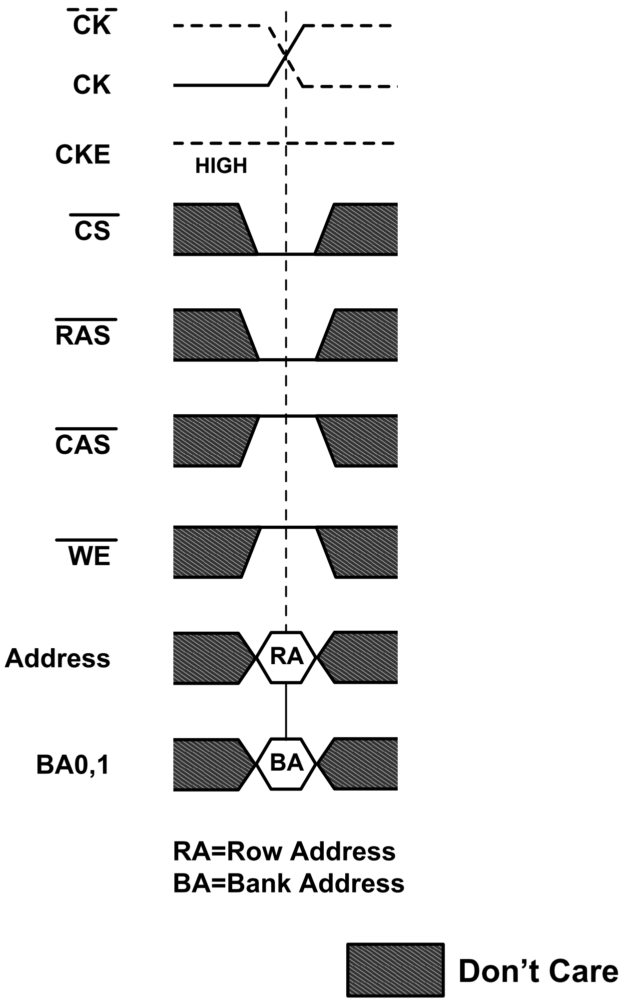


Figure 7. tRCD and tRRD Definition

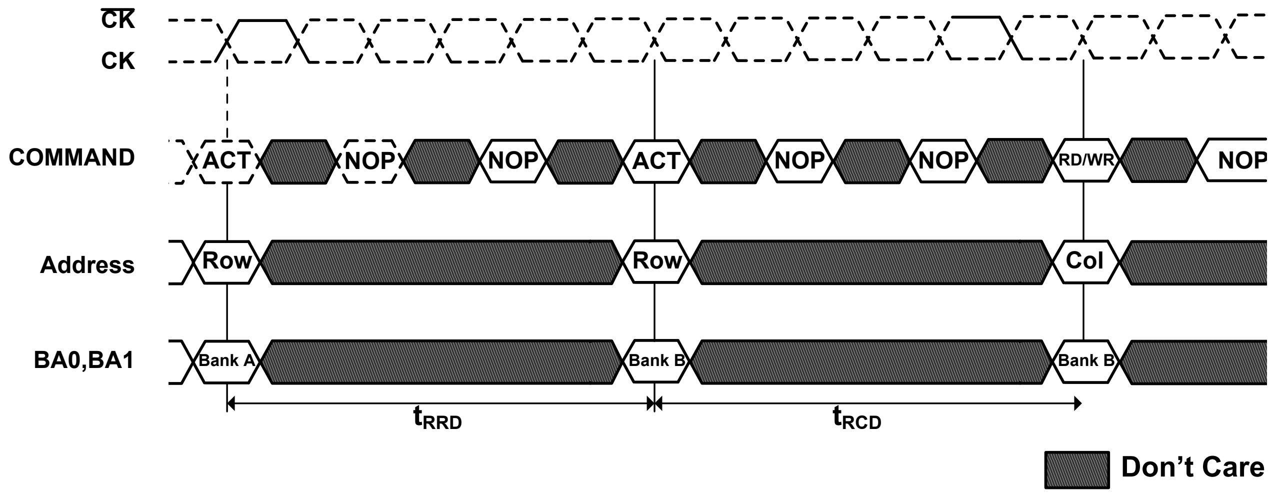


Figure 8. READ Command

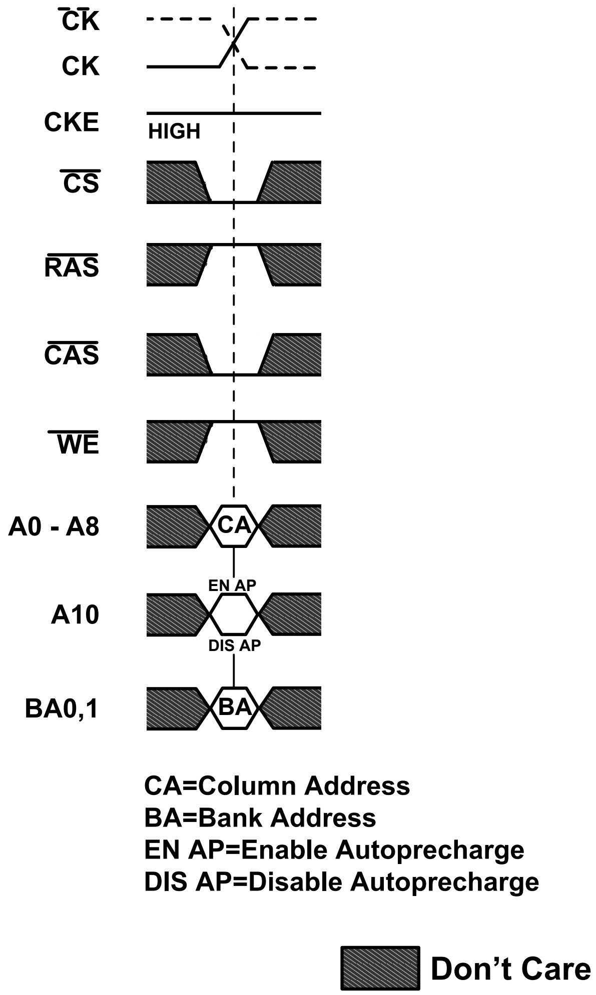


Figure 9. Read Burst Required CAS Latencies (CL=2)

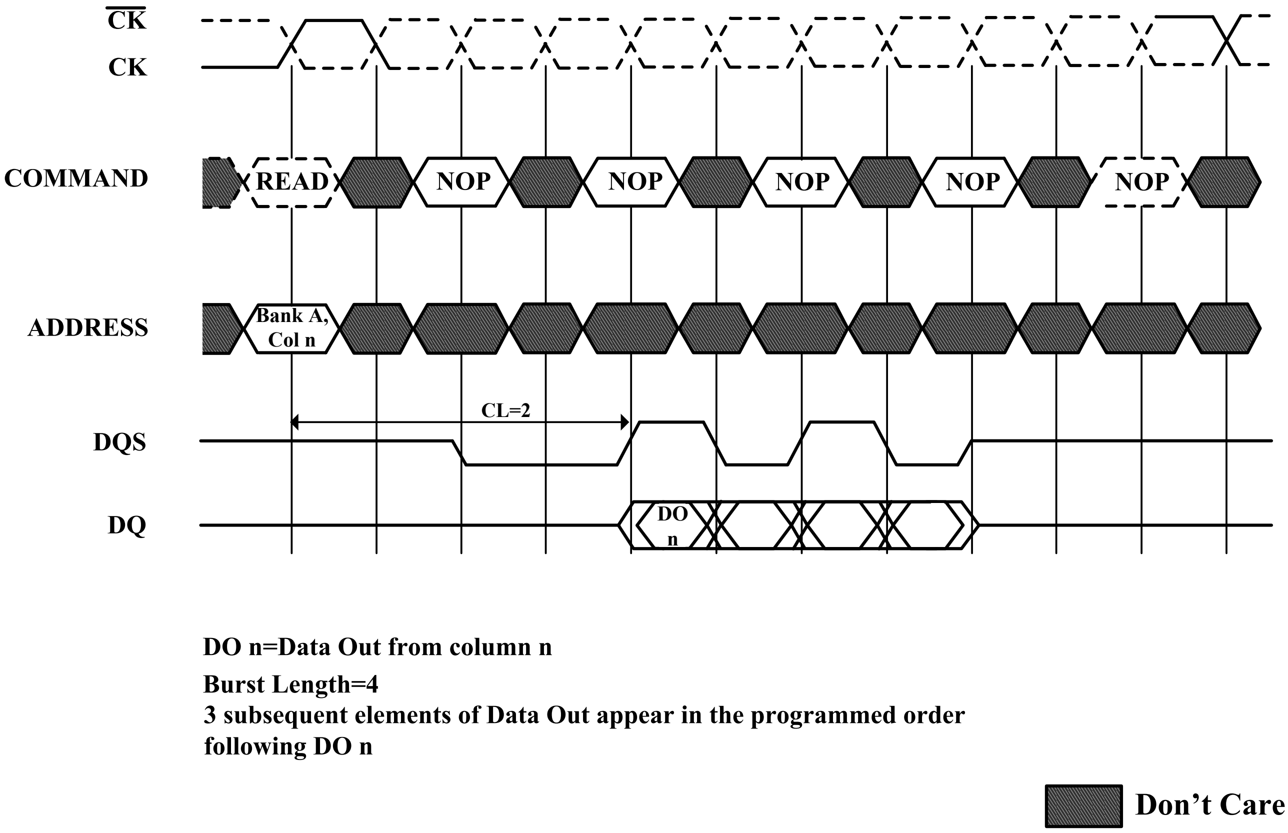


Figure 10. Read Burst Required CAS Latencies (CL=2.5)

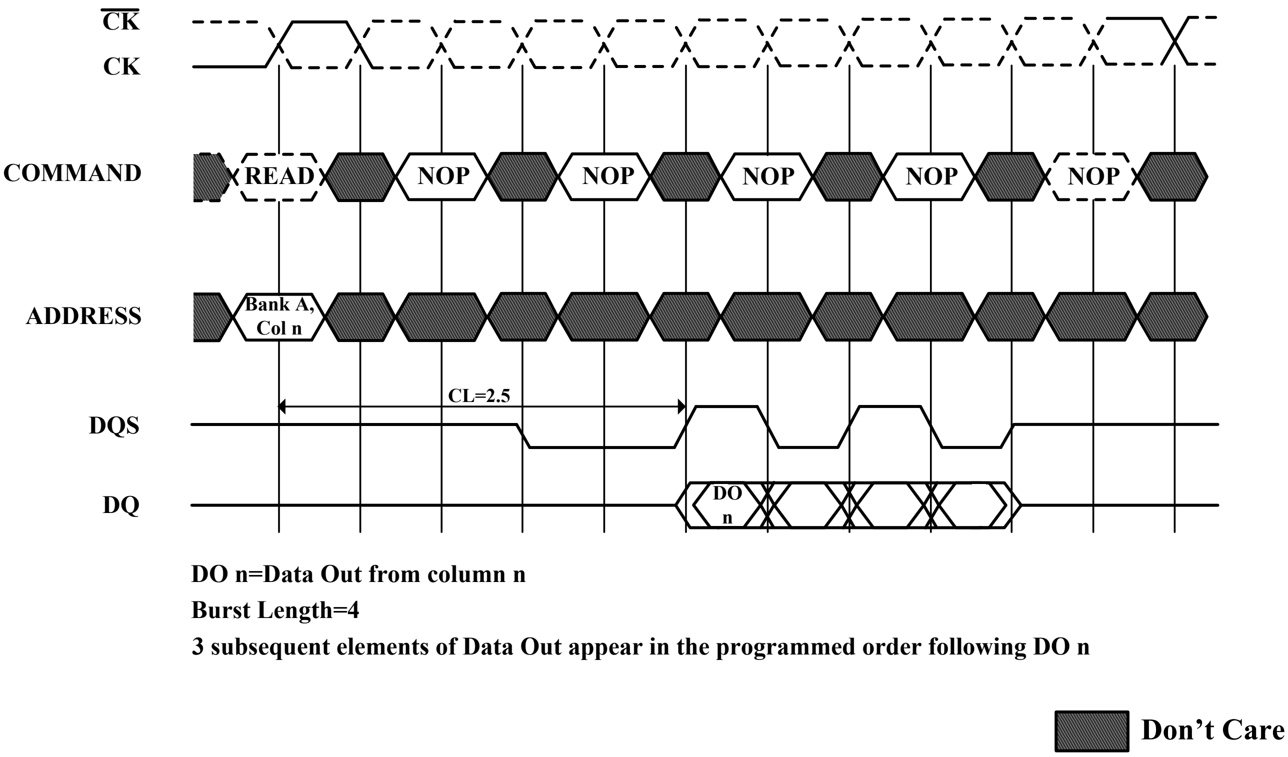


Figure 11. Read Burst Required CAS Latencies (CL=3)

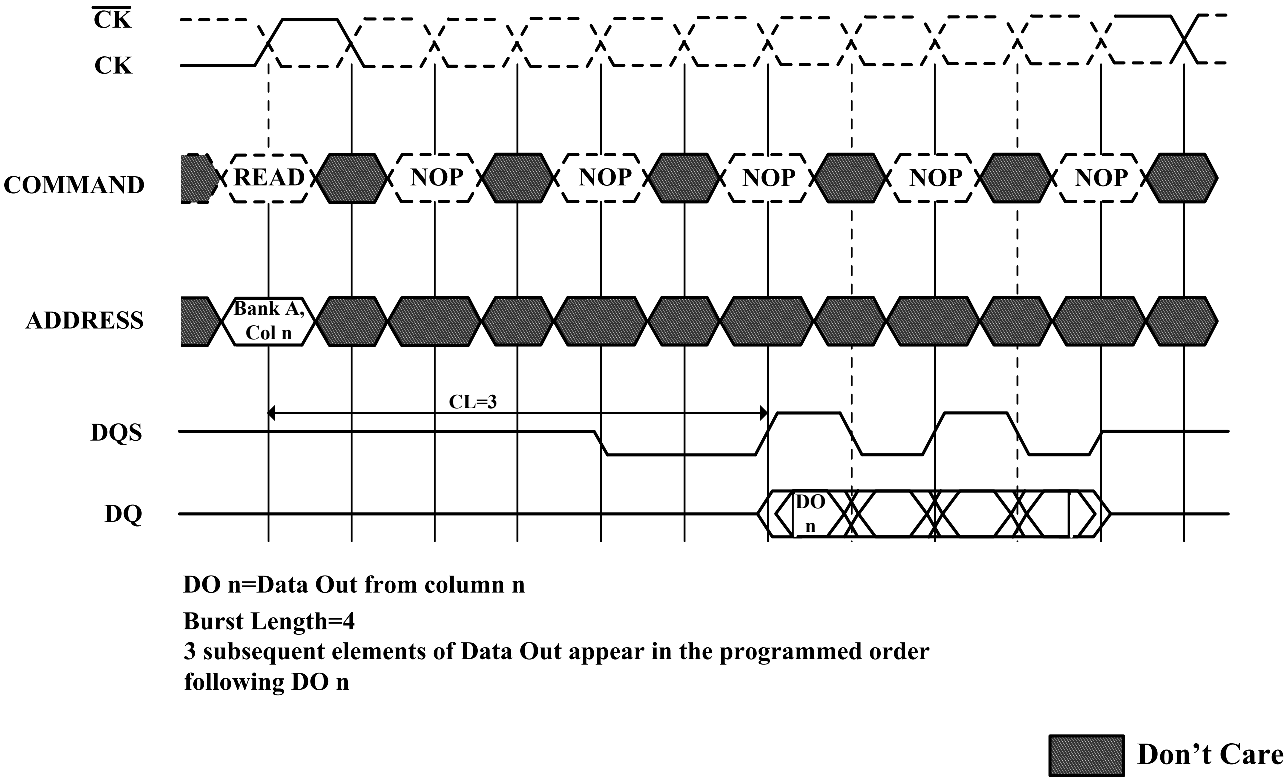
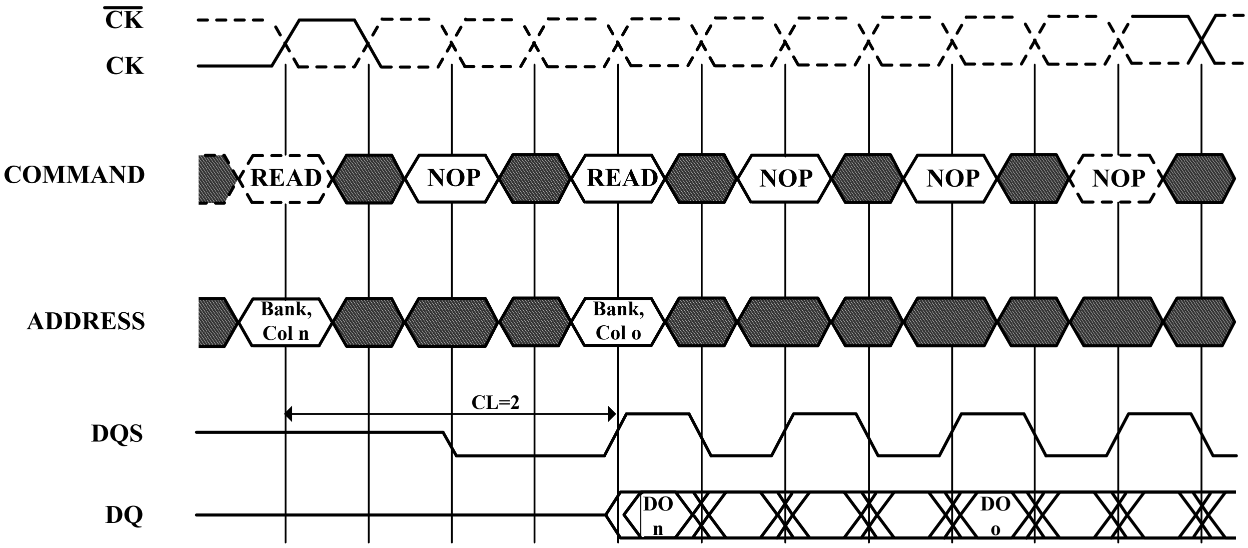


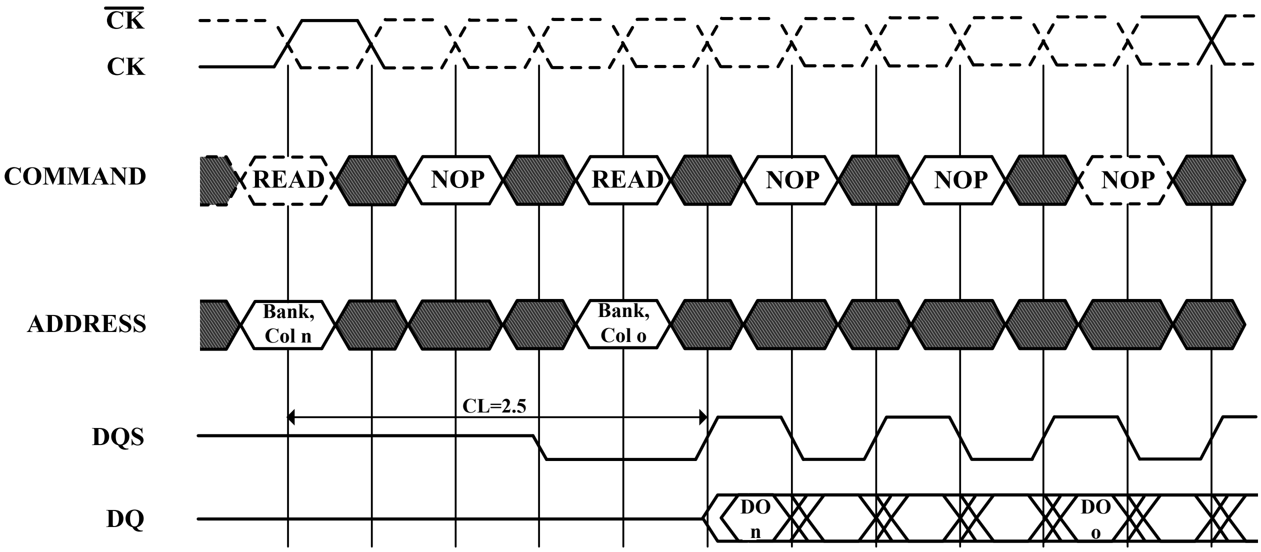
Figure 12. Consecutive Read Bursts Required CAS Latencies (CL=2)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

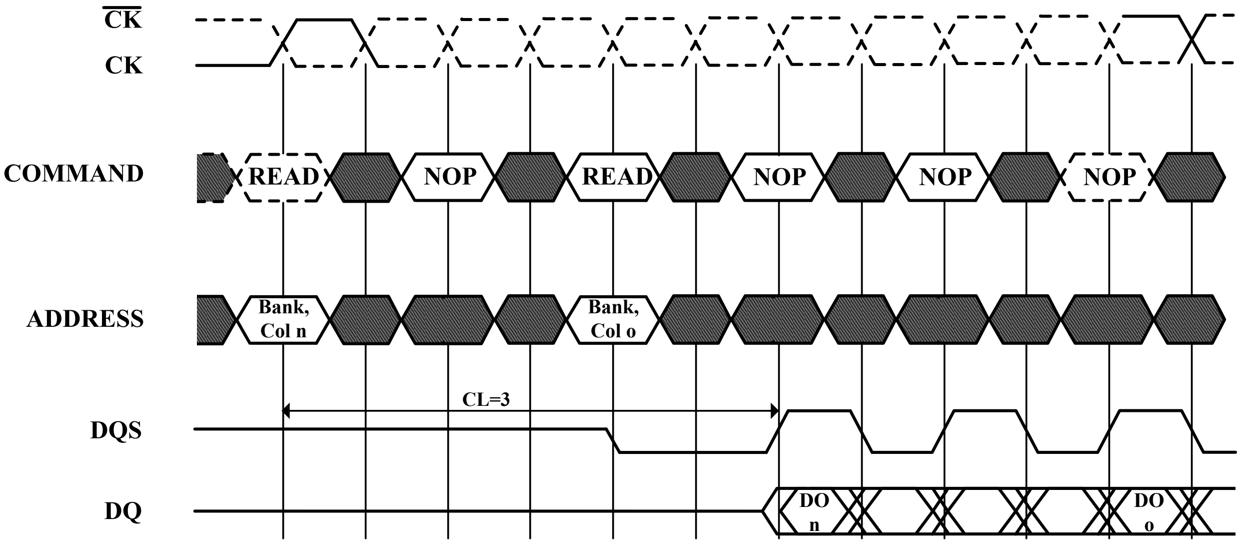
Don’t Care

Figure 13. Consecutive Read Bursts Required CAS Latencies (CL=2.5)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

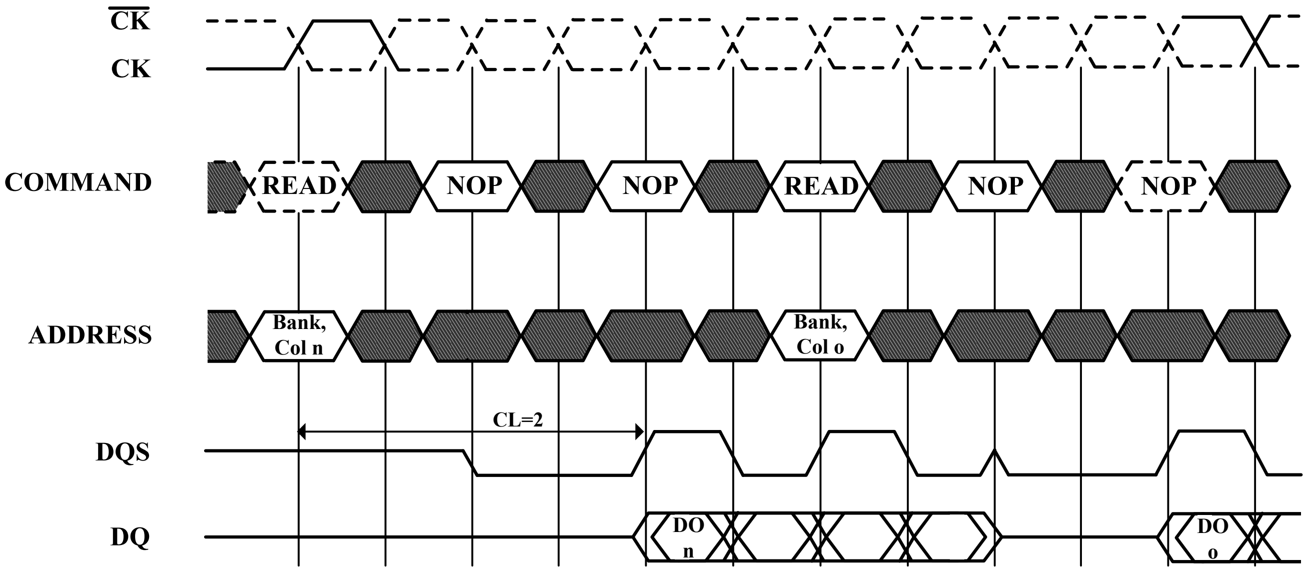
Figure 14. Consecutive Read Bursts Required CAS Latencies (CL=3)



DO n (or o)=Data Out from column n (or column o)
Burst Length=4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO o
Read commands shown must be to the same device

Don't Care

Figure 15. Non-Consecutive Read Bursts Required CAS Latencies (CL=2)



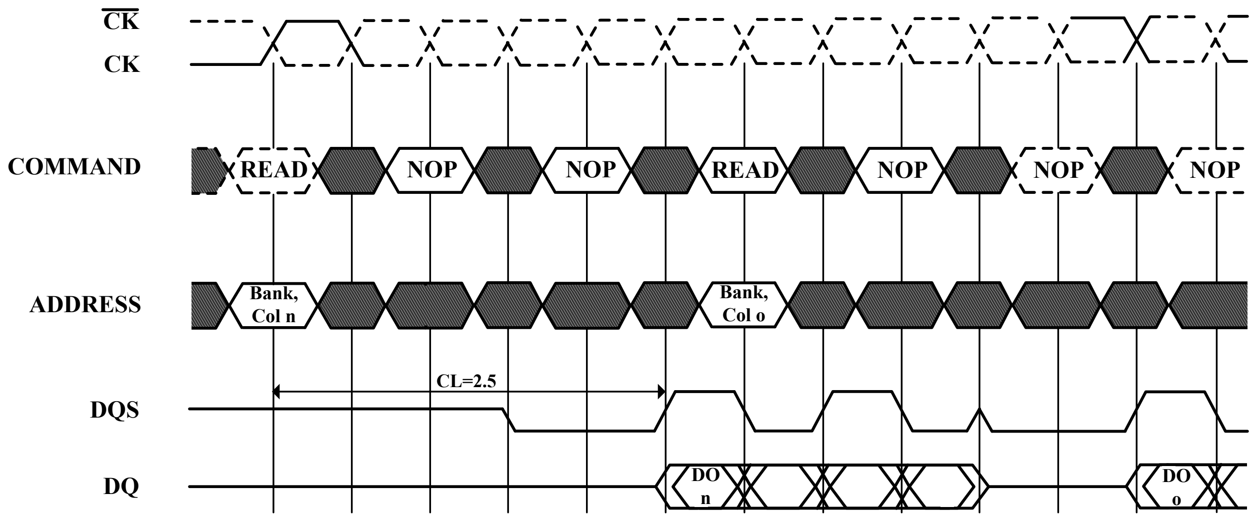
DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

Don't Care

Figure 16. Non-Consecutive Read Bursts Required CAS Latencies (CL=2.5)



DO n (or o)=Data Out from column n (or column o)

Burst Length=4

3 subsequent elements of Data Out appear in the programmed order following DO n (and following DO o)

Don't Care

Figure 17. Non-Consecutive Read Bursts Required CAS Latencies (CL=3)

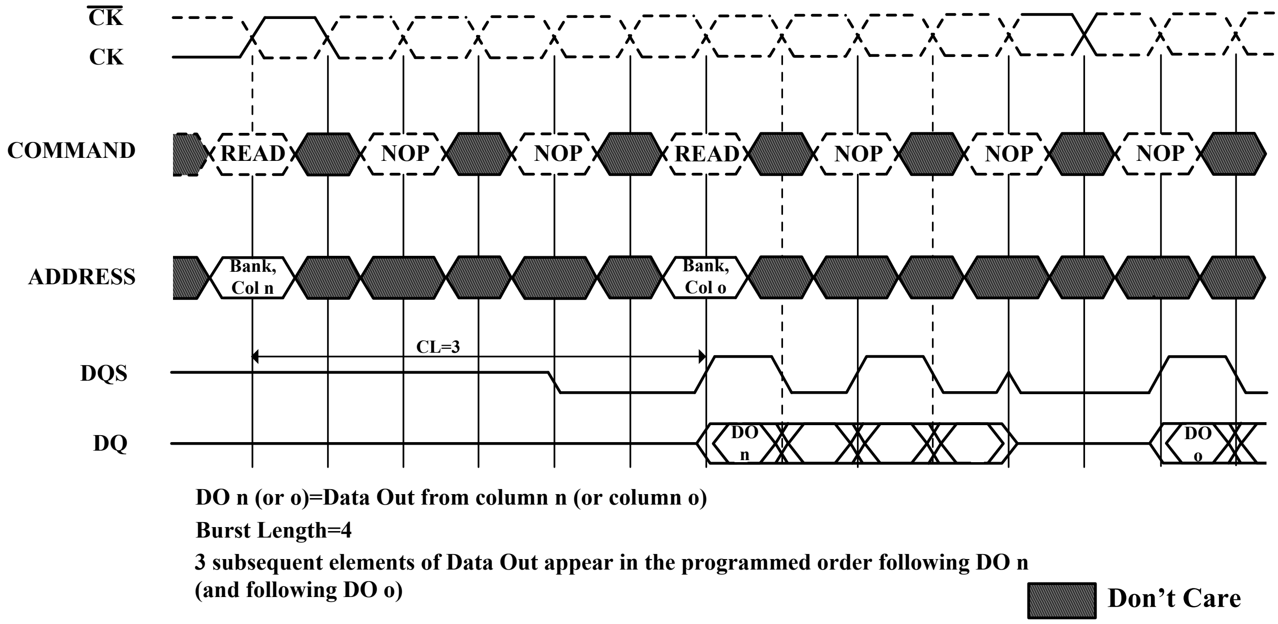
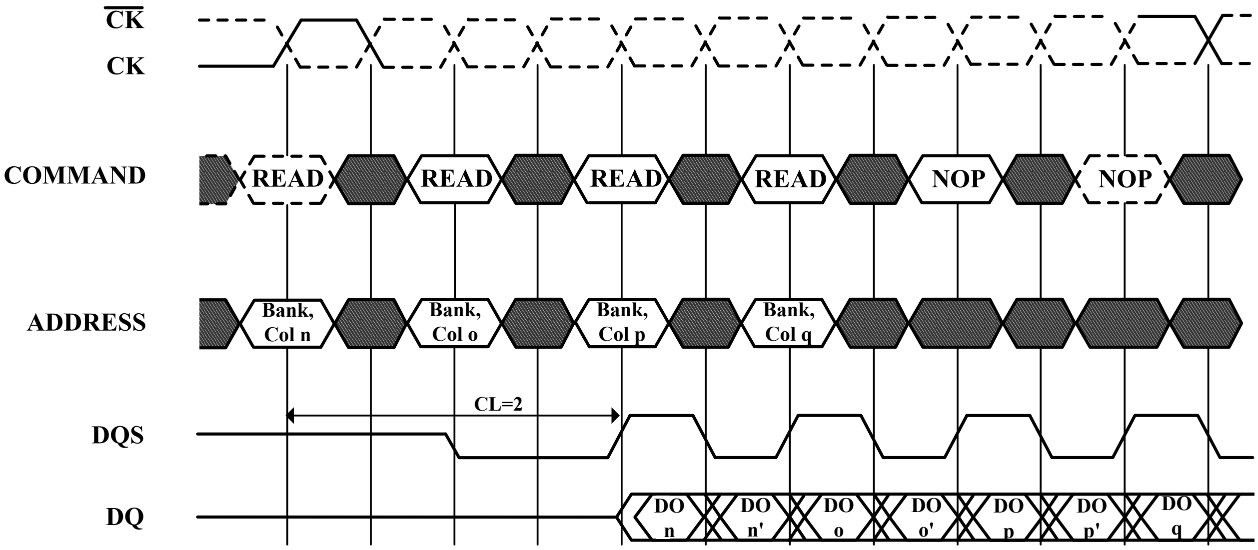


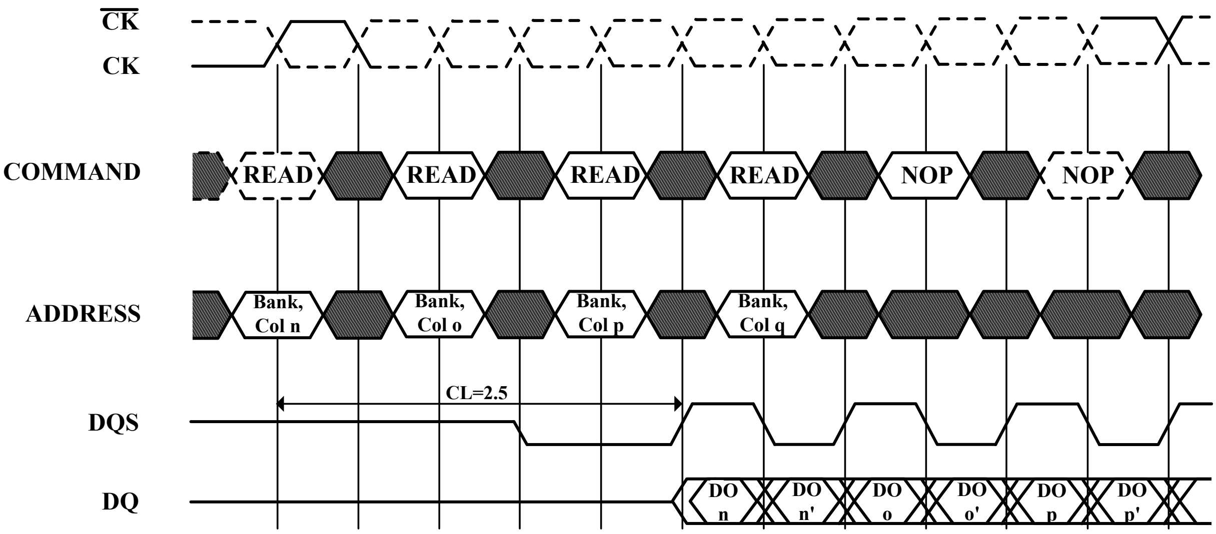
Figure 18. Random Read Accesses Required CAS Latencies (CL=2)



DO n, etc. =Data Out from column n, etc.
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order
Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted
Reads are to active rows in any banks

Don't Care

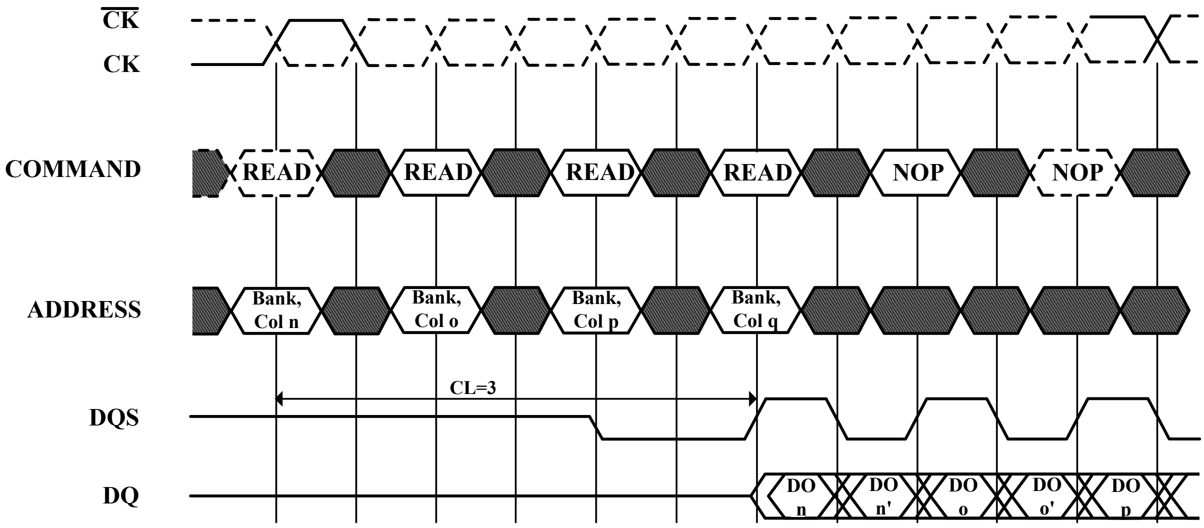
Figure 19. Random Read Accesses Required CAS Latencies (CL=2.5)



DO n, etc. =Data Out from column n, etc.
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order
Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted
Reads are to active rows in any banks

Don't Care

Figure 20. Random Read Accesses Required CAS Latencies (CL=3)



DO n, etc. =Data Out from column n, etc.

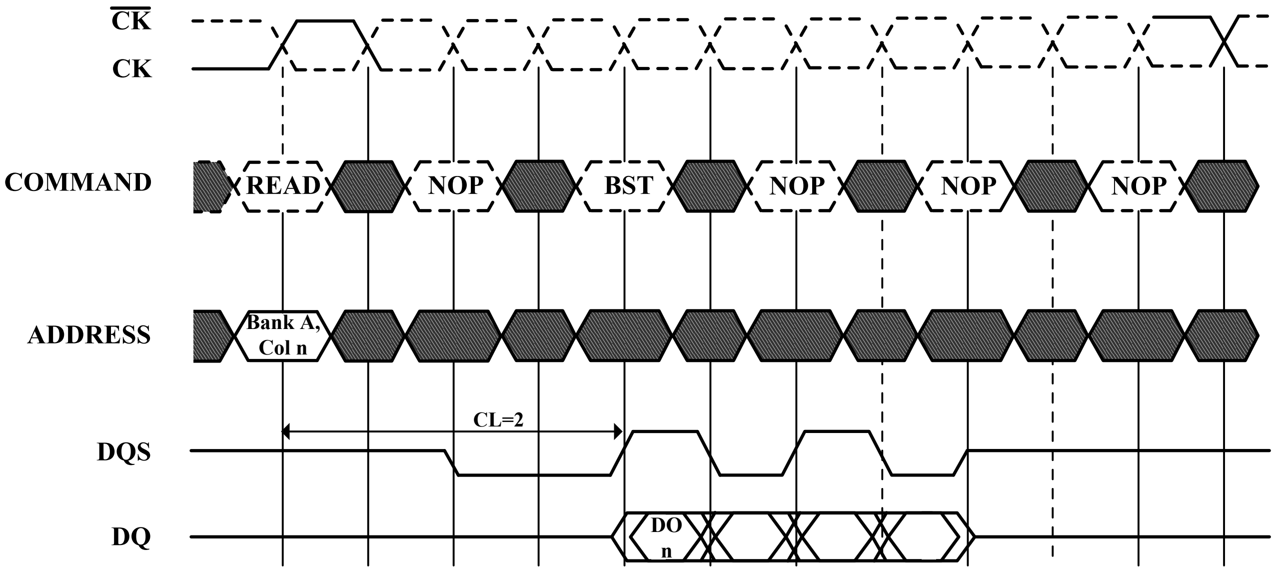
n', etc. =the next Data Out following DO n, etc. according to the programmed burst order

Burst Length=2,4 or 8 in cases shown. If burst of 4 or 8, the burst is interrupted

Reads are to active rows in any banks

Don't Care

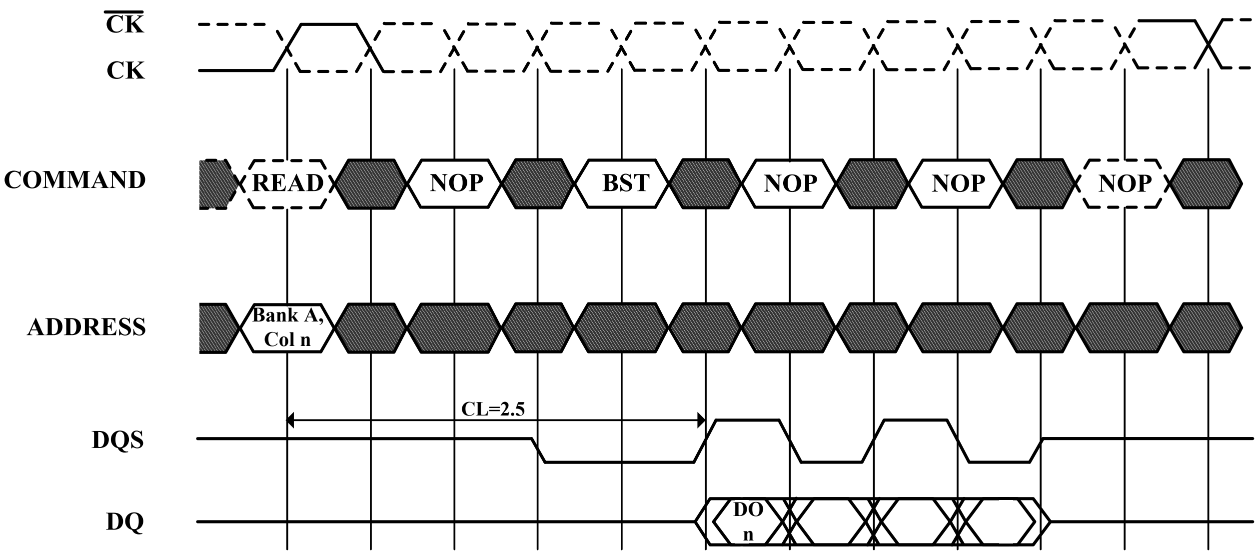
Figure 21. Terminating a Read Burst Required CAS Latencies (CL=2)



DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

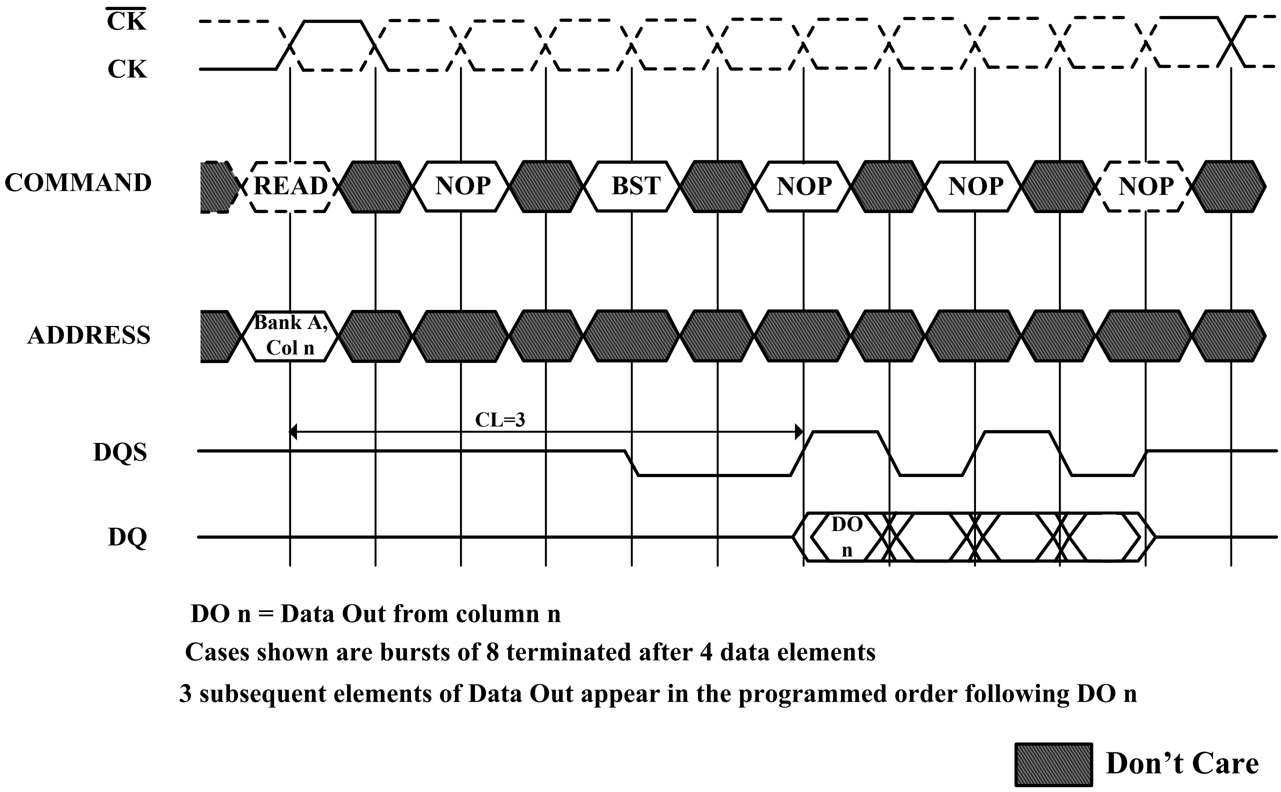
Figure 22. Terminating a Read Burst Required CAS Latencies (CL=2.5)



DO n = Data Out from column n
Cases shown are bursts of 8 terminated after 4 data elements
3 subsequent elements of Data Out appear in the programmed order following DO n

Don't Care

Figure 23. Terminating a Read Burst Required CAS Latencies (CL=3)

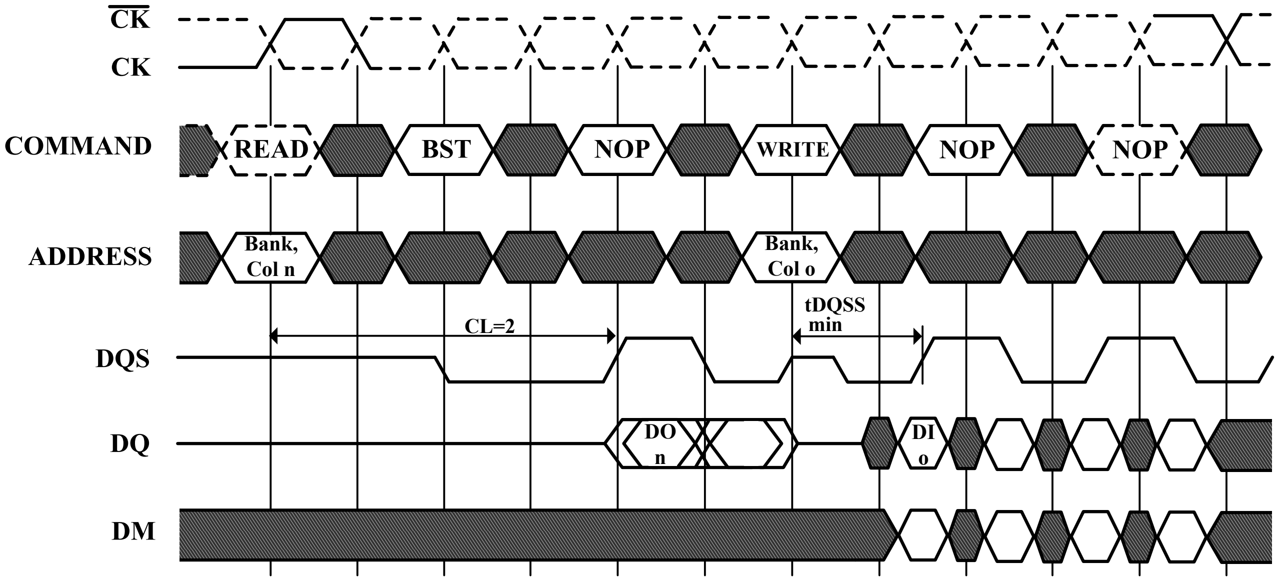


DO n = Data Out from column n

Cases shown are bursts of 8 terminated after 4 data elements

3 subsequent elements of Data Out appear in the programmed order following DO n

Figure 24. Read to Write Required CAS Latencies (CL=2)



DO n (or o)= Data Out from column n (or column o)

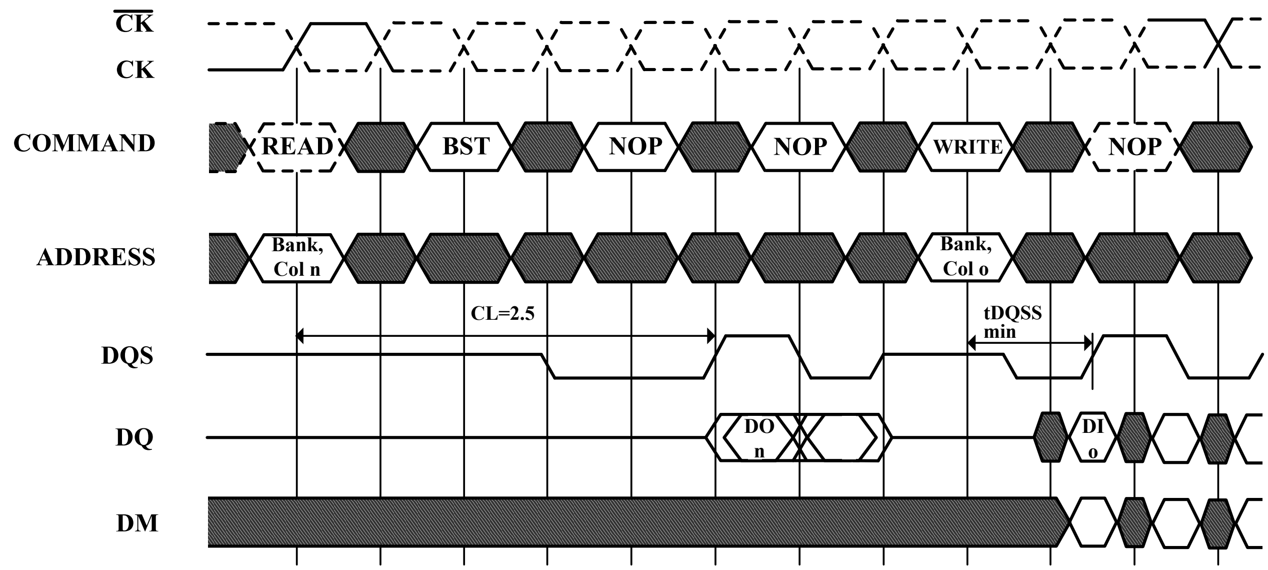
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

Don't Care

Figure 25. Read to Write Required CAS Latencies (CL=2.5)



DO n (or o)= Data Out from column n (or column o)

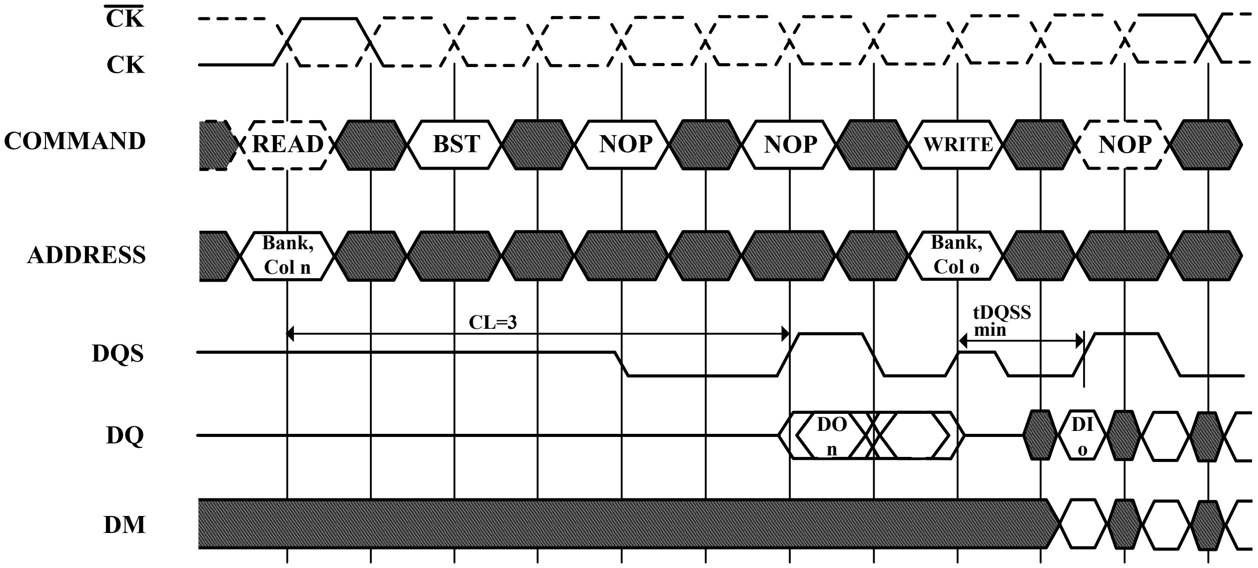
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

Don't Care

Figure 26. Read to Write Required CAS Latencies (CL=3)



DO n (or o)= Data Out from column n (or column o)

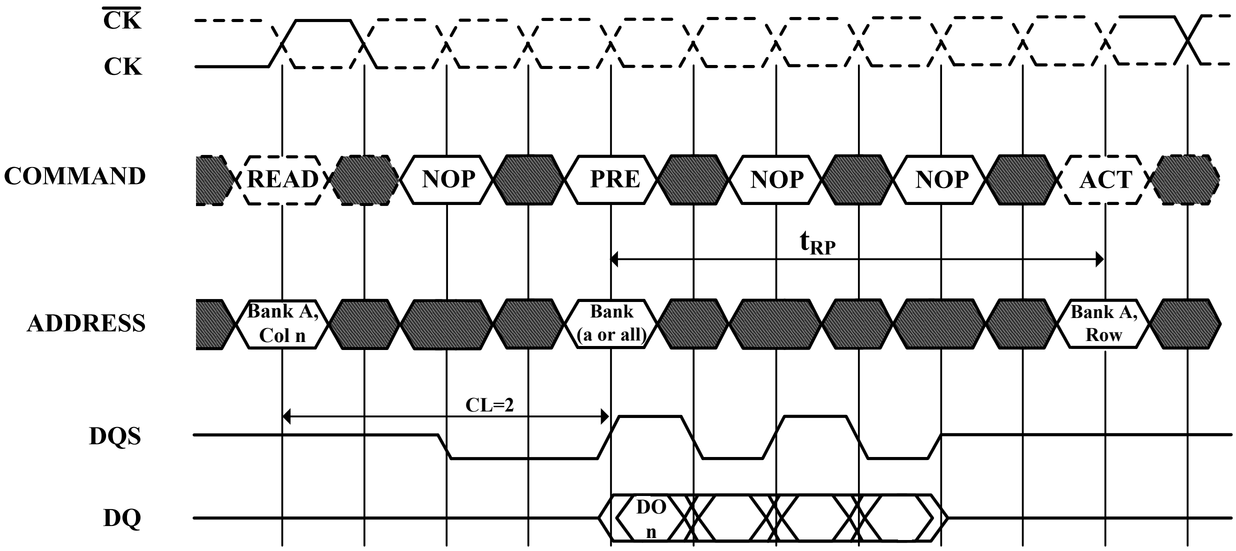
Burst Length= 4 in the cases shown (applies for bursts of 8 as well; if burst length is 2, the BST command shown can be NOP)

1 subsequent element of Data Out appears in the programmed order following DO n

Data in elements are applied following DI o in the programmed order

Don't Care

Figure 27. Read to Precharge Required CAS Latencies (CL=2)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

3 subsequent elements of Data Out appear in the programmed order following DO n

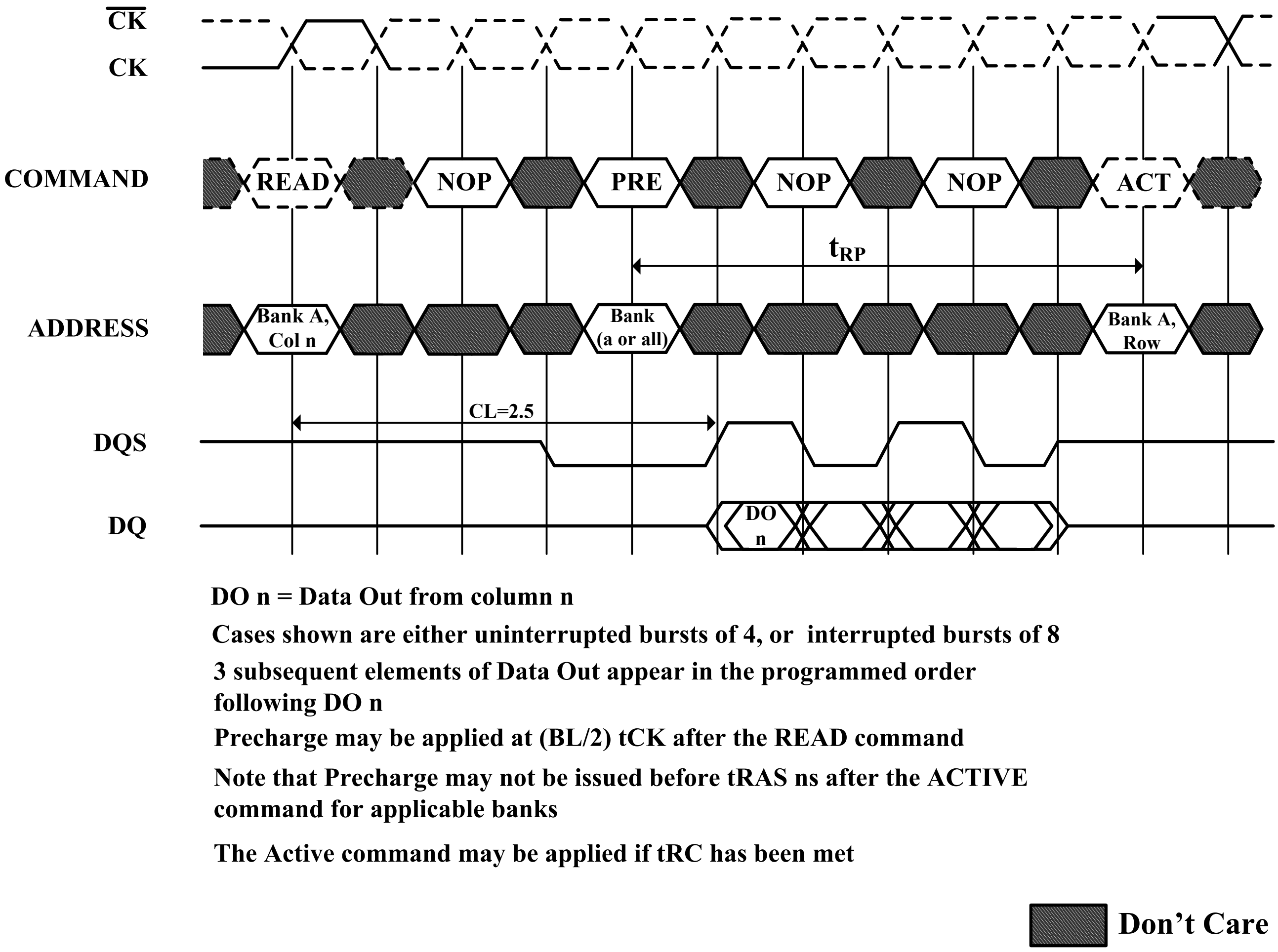
Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met

Don't Care

Figure 28. Read to Precharge Required CAS Latencies (CL=2.5)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

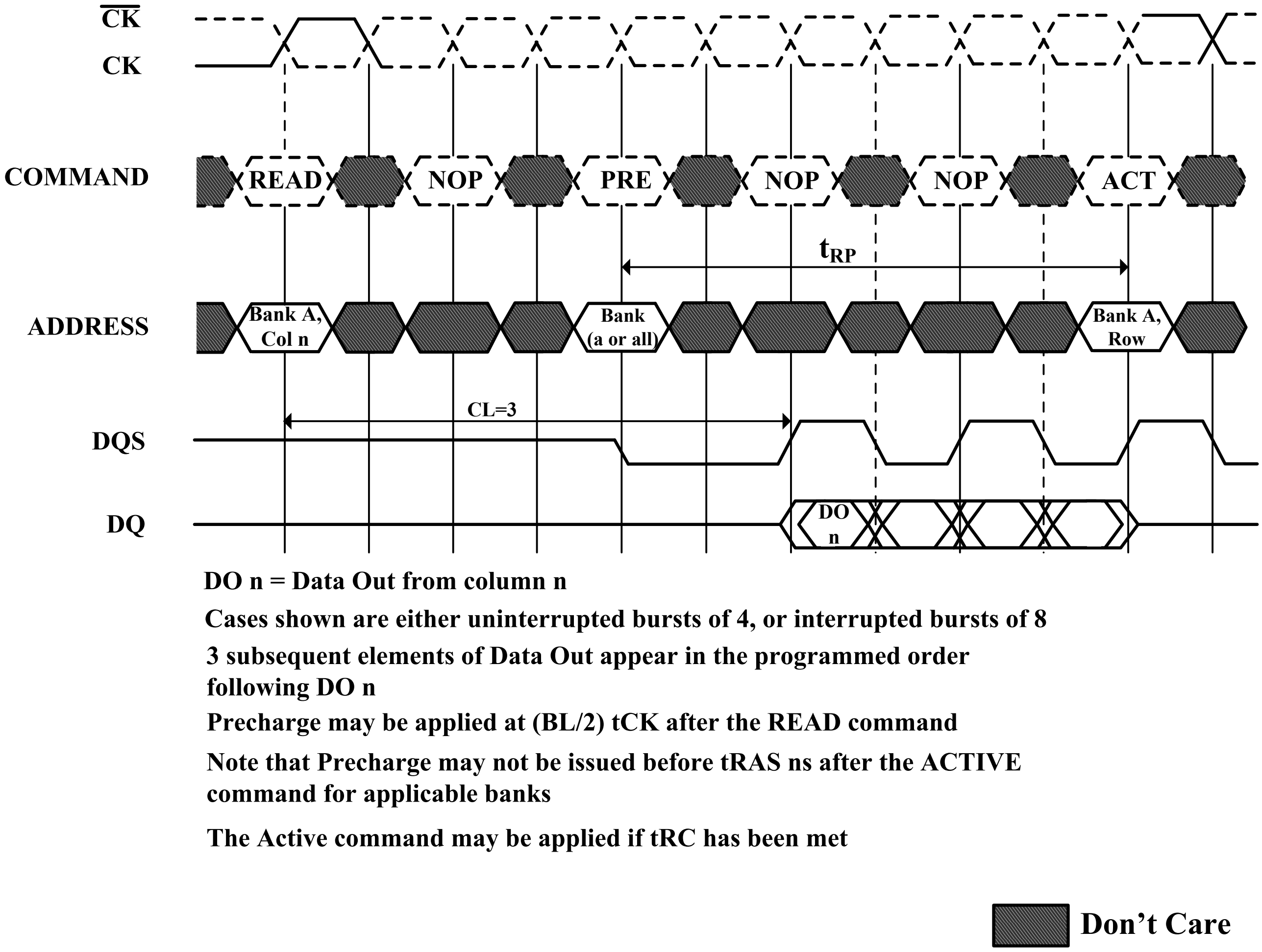
3 subsequent elements of Data Out appear in the programmed order following DO n

Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met

Figure 29. Read to Precharge Required CAS Latencies (CL=3)



DO n = Data Out from column n

Cases shown are either uninterrupted bursts of 4, or interrupted bursts of 8

3 subsequent elements of Data Out appear in the programmed order following DO n

Precharge may be applied at (BL/2) tCK after the READ command

Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

The Active command may be applied if tRC has been met

Figure 30. Write Command

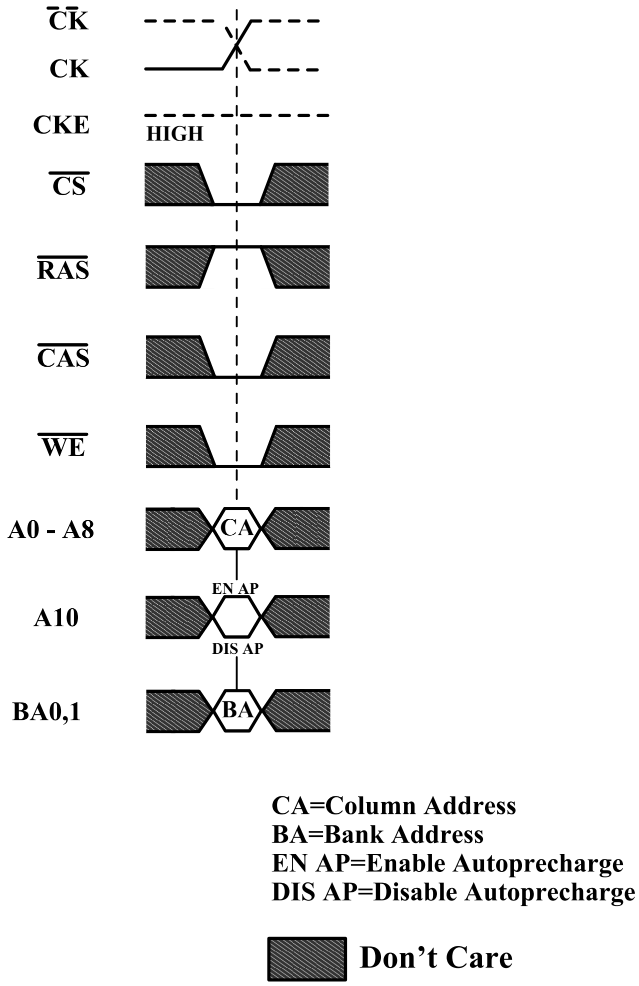
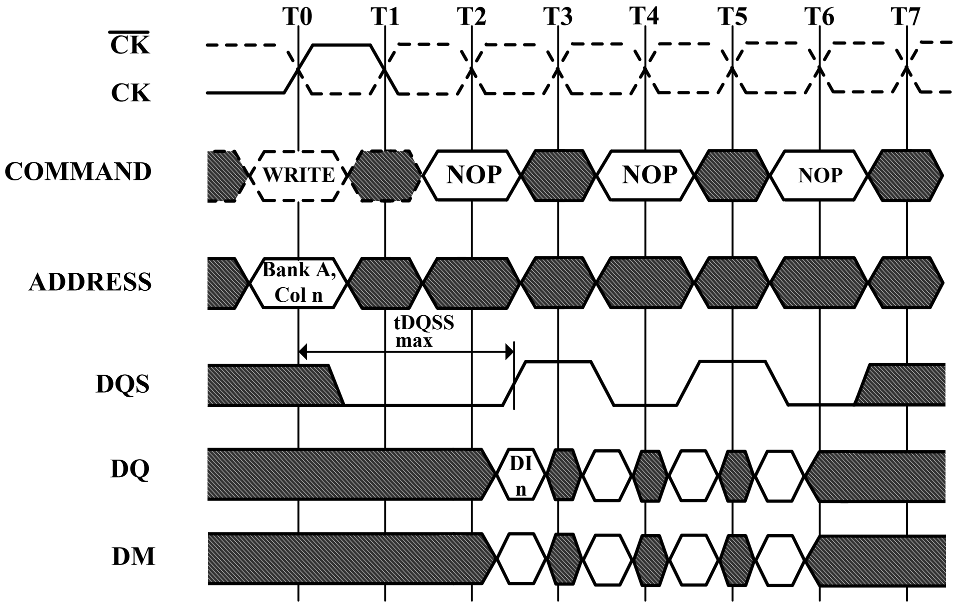


Figure 31. Write Max DQSS



DI n = Data In for column n

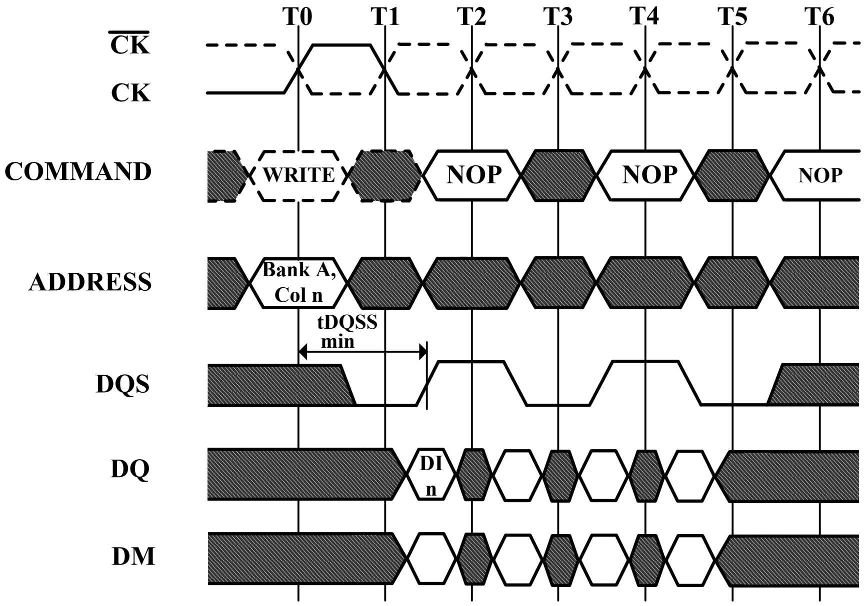
3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Don't Care

Figure 32. Write Min DQSS



DI n = Data In for column n

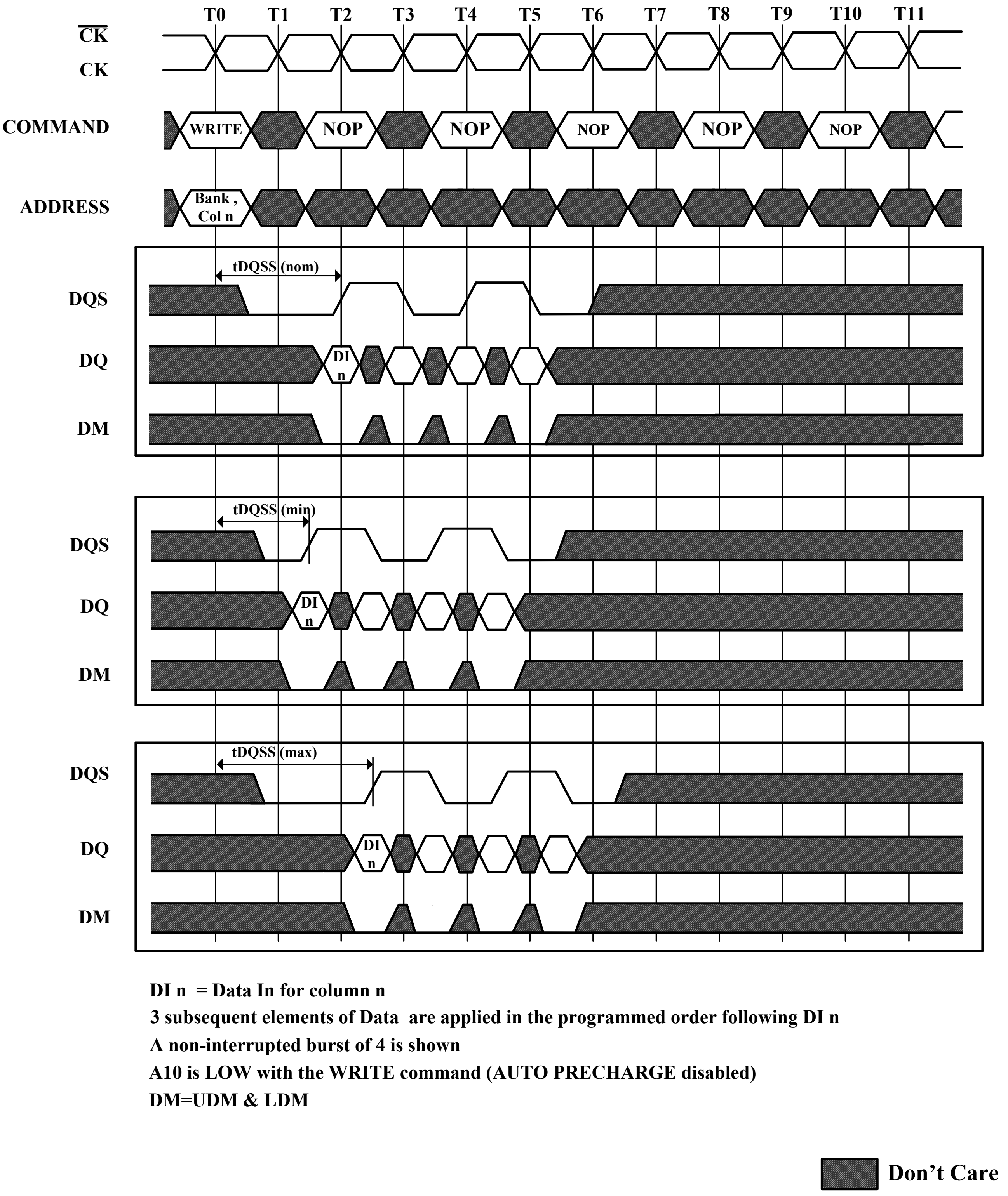
3 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

Don't Care

Figure 33. Write Burst Nom, Min, and Max tDQSS



DI n = Data In for column n

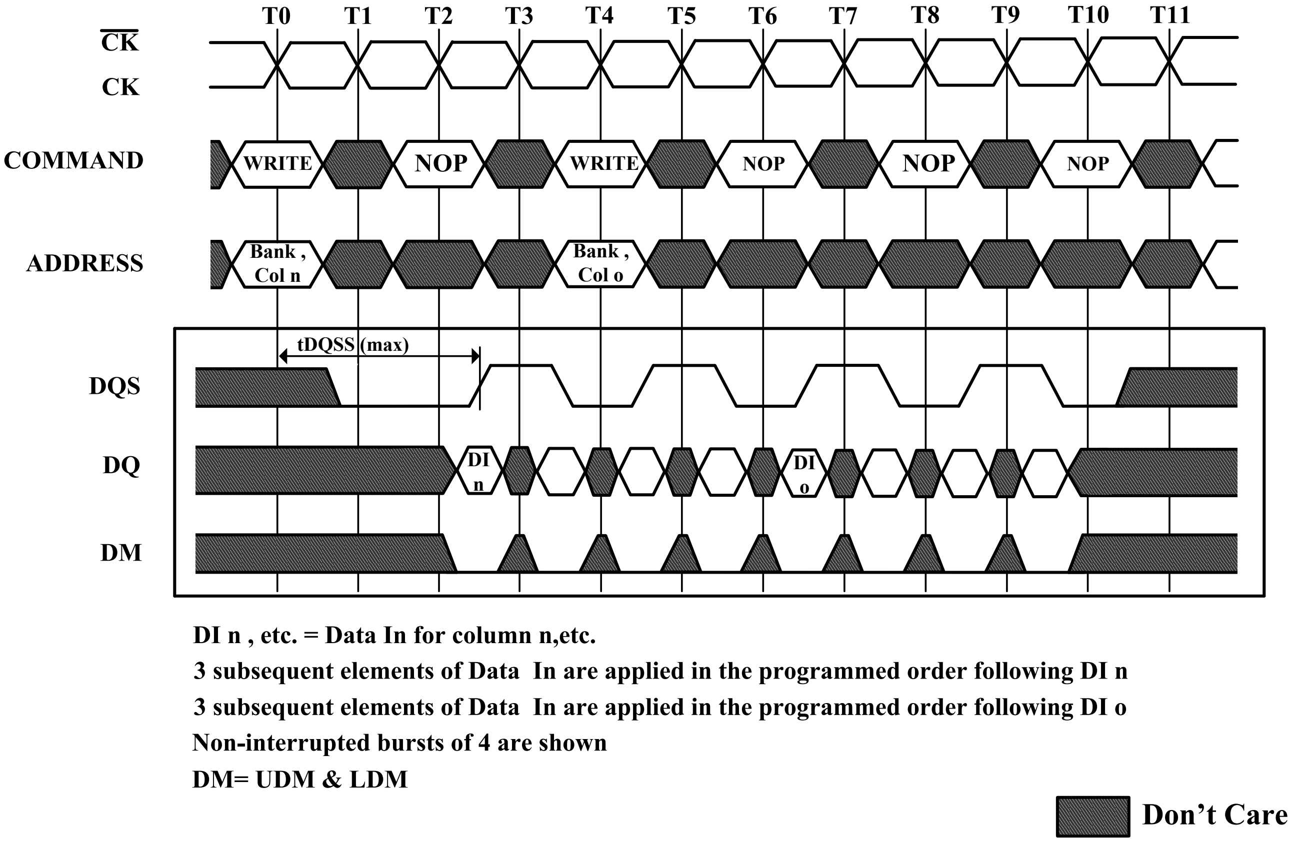
3 subsequent elements of Data are applied in the programmed order following DI n

A non-interrupted burst of 4 is shown

A10 is LOW with the WRITE command (AUTO PRECHARGE disabled)

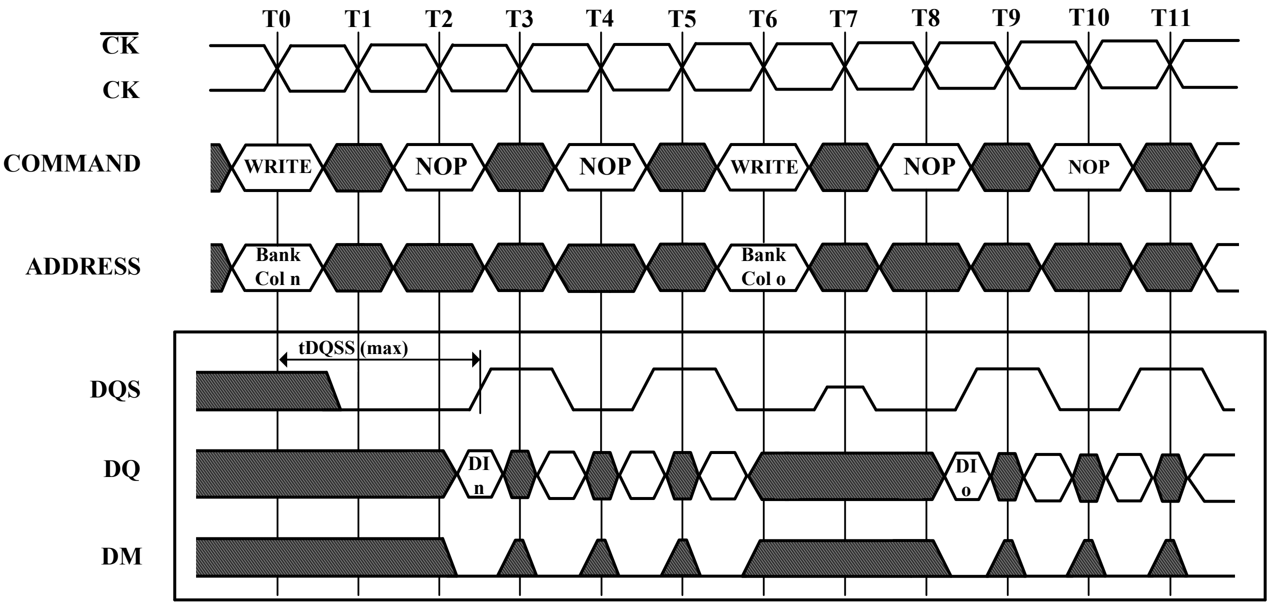
DM=UDM & LDM

Figure 34. Write to Write Max tDQSS



DI n , etc. = Data In for column n,etc.
3 subsequent elements of Data In are applied in the programmed order following DI n
3 subsequent elements of Data In are applied in the programmed order following DI o
Non-interrupted bursts of 4 are shown
DM= UDM & LDM

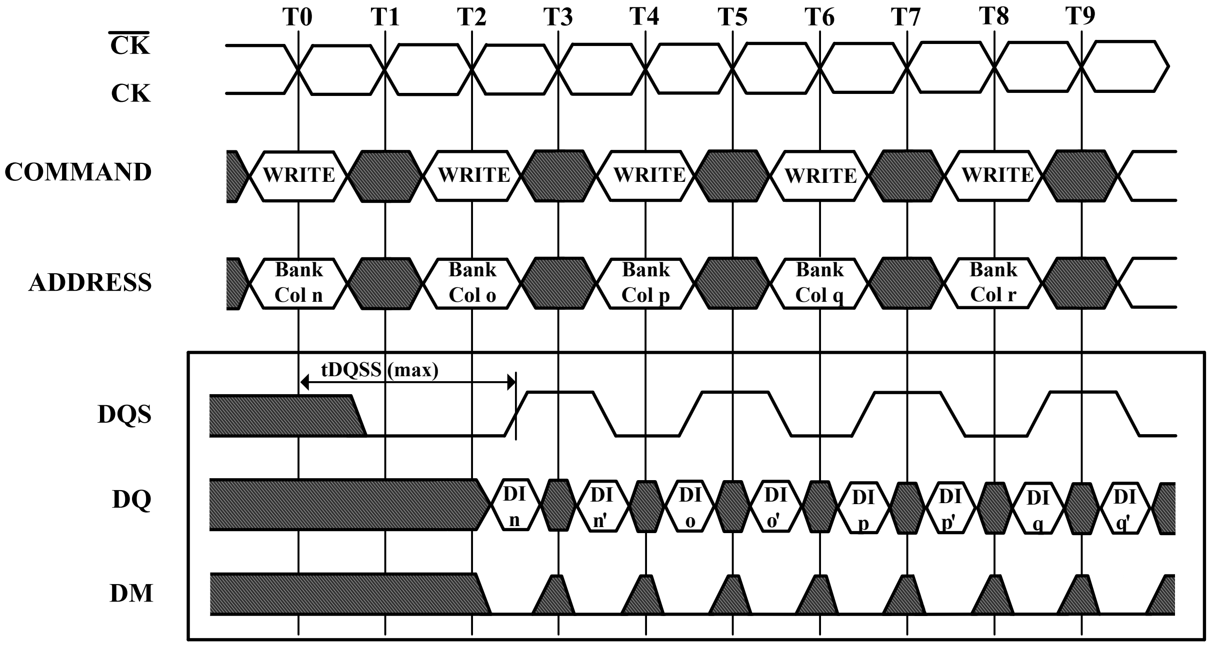
Figure 35. Write to Write Max tDQSS, Non Consecutive



DI n, etc. = Data In for column n, etc.
3 subsequent elements of Data In are applied in the programmed order following DI n
3 subsequent elements of Data In are applied in the programmed order following DI o
Non-interrupted bursts of 4 are shown
DM= UDM & LDM

Don't Care

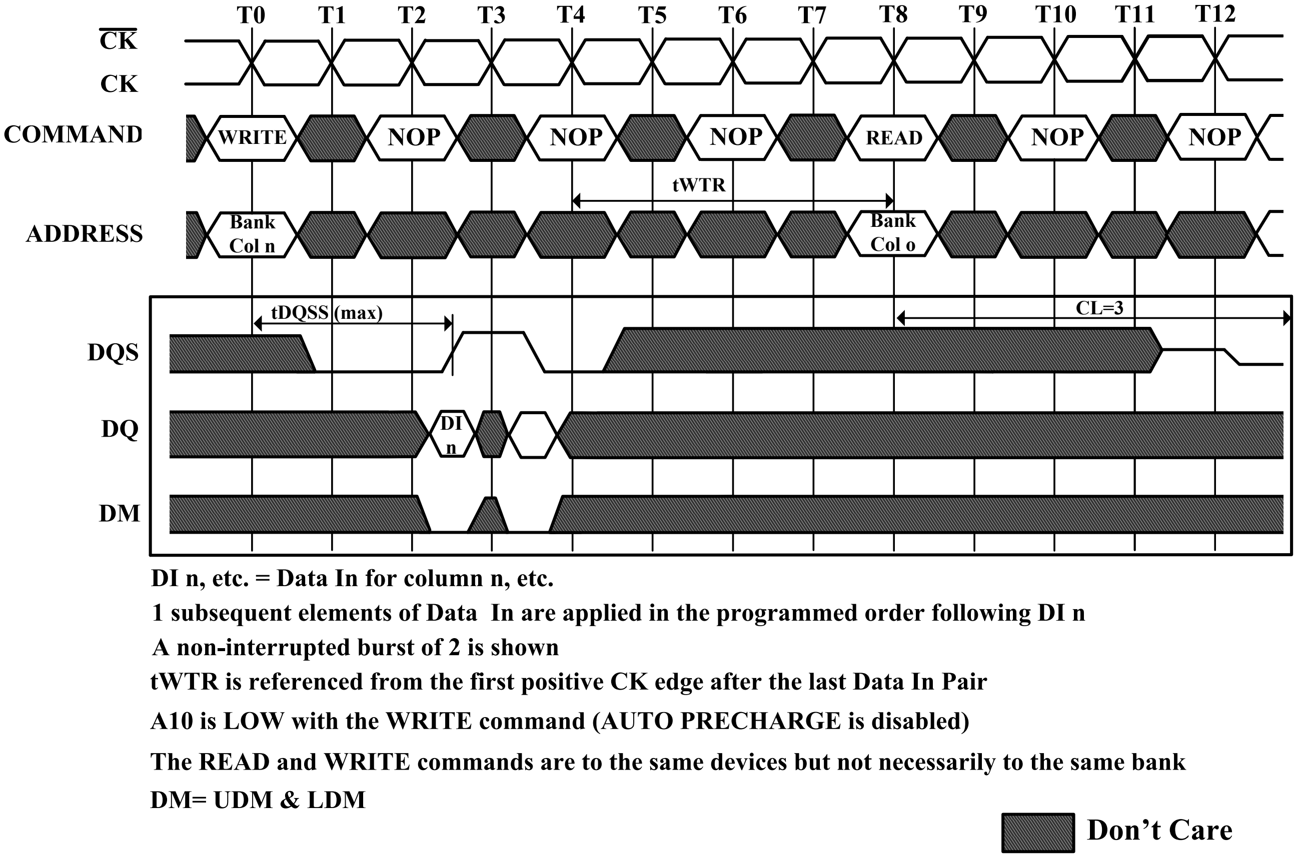
Figure 36. Random Write Cycles Max tDQSS



DI n, etc. = Data In for column n, etc.
n', etc. = the next Data In following DI n, etc. according to the programmed burst order
Programmed Burst Length 2, 4, or 8 in cases shown
If burst of 4 or 8, the burst would be truncated
Each WRITE command may be to any bank and may be to the same or different devices
DM= UDM & LDM

Don't Care

Figure 37. Write to Read Max tDQSS Non Interrupting



DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 2 is shown

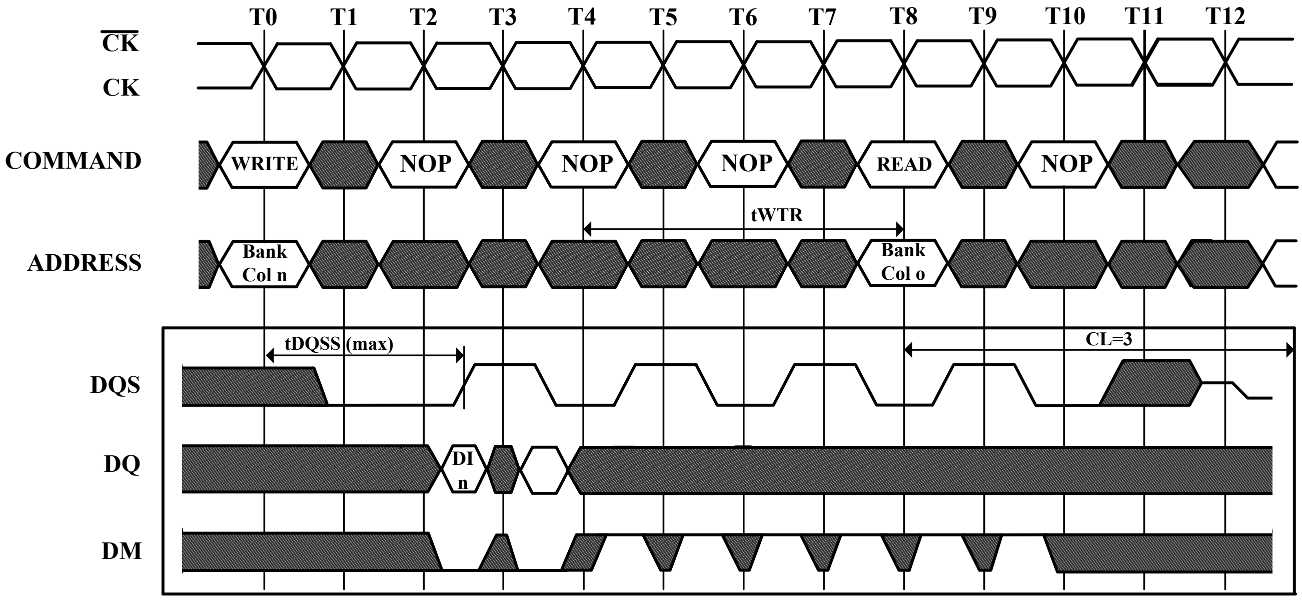
tWTR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= UDM & LDM

Figure 38. Write to Read Max tDQSS Interrupting



DI n, etc. = Data In for column n, etc.

1 subsequent elements of Data In are applied in the programmed order following DI n

An interrupted burst of 8 is shown, 2 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair

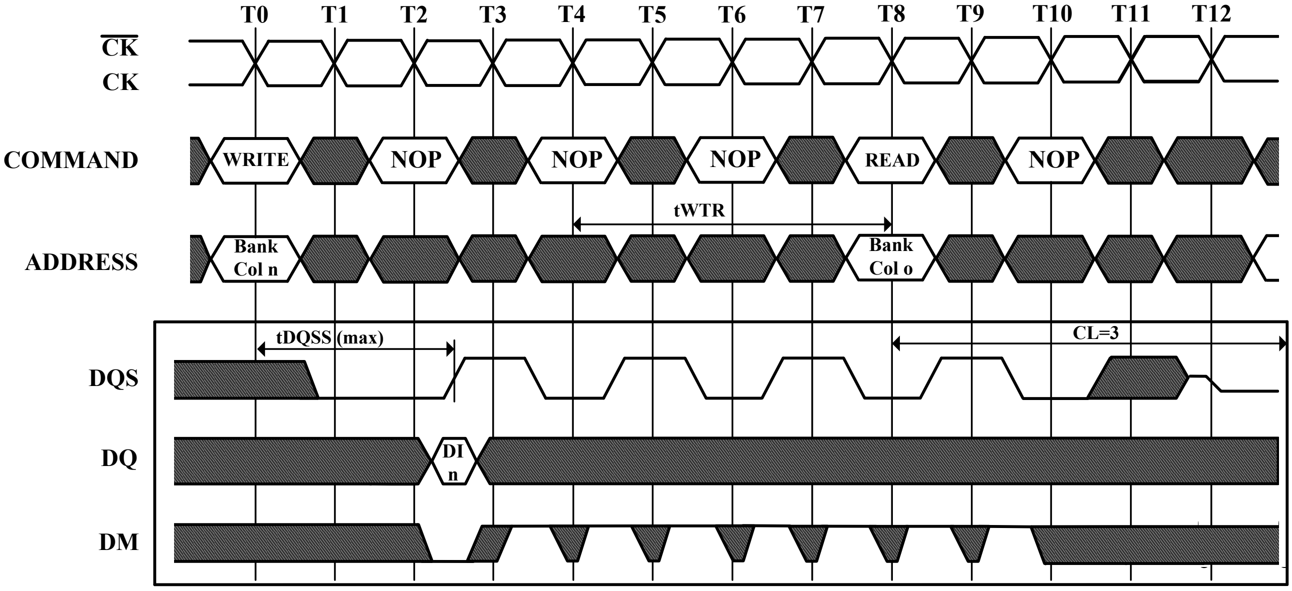
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= UDM & LDM

Don't Care

Figure 39. Write to Read Max tDQSS, ODD Number of Data, Interrupting



DI n = Data In for column n

An interrupted burst of 8 is shown, 1 data elements are written

tWTR is referenced from the first positive CK edge after the last Data In Pair (not the last desired Data In element)

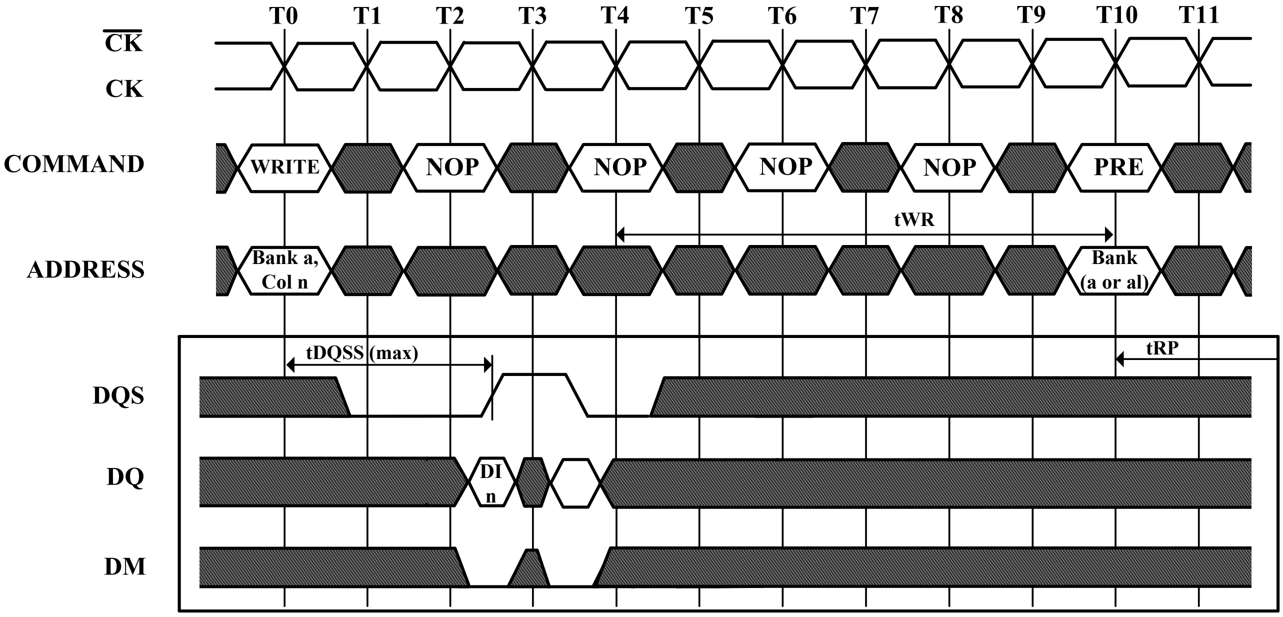
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

The READ and WRITE commands are to the same devices but not necessarily to the same bank

DM= LDM & UDM

Don't Care

Figure 40. Write to Precharge Max tDQSS, NON- Interrupting



DI n = Data In for column n

1 subsequent elements of Data In are applied in the programmed order following DI n

A non-interrupted burst of 2 is shown

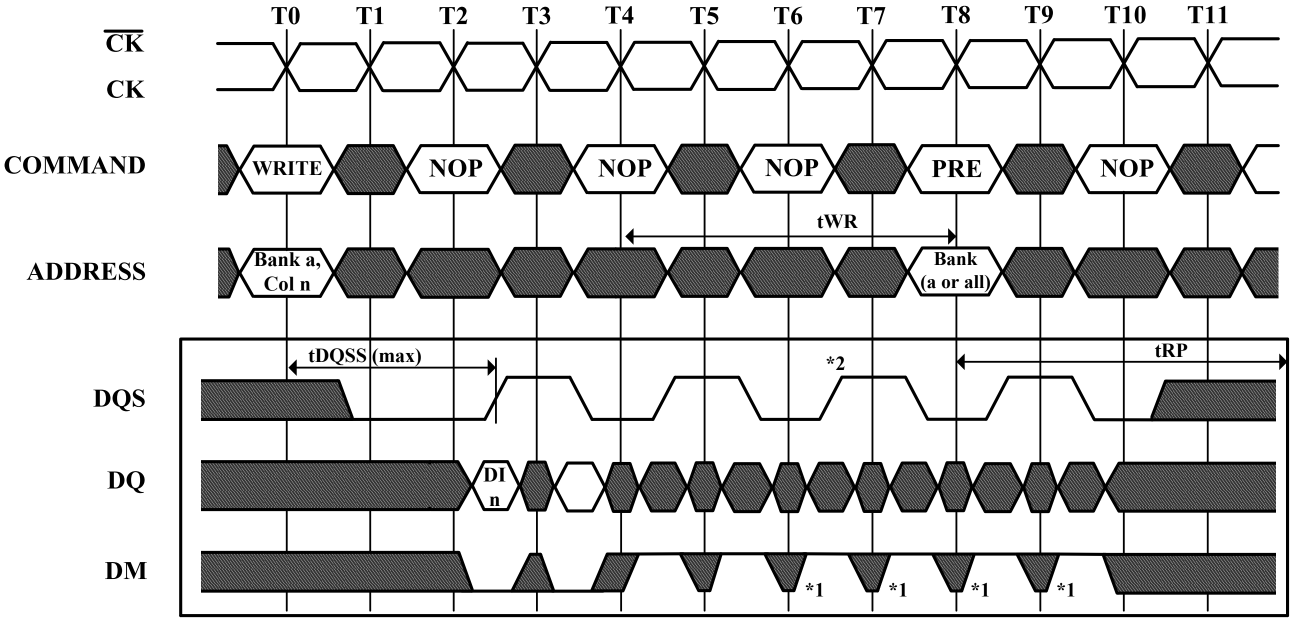
tWR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

DM= UDM & LDM

Don't Care

Figure 41. Write to Precharge Max tDQSS, Interrupting



DI n = Data In for column n

An interrupted burst of 4 or 8 is shown, 2 data elements are written

tWR is referenced from the first positive CK edge after the last Data In Pair

A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)

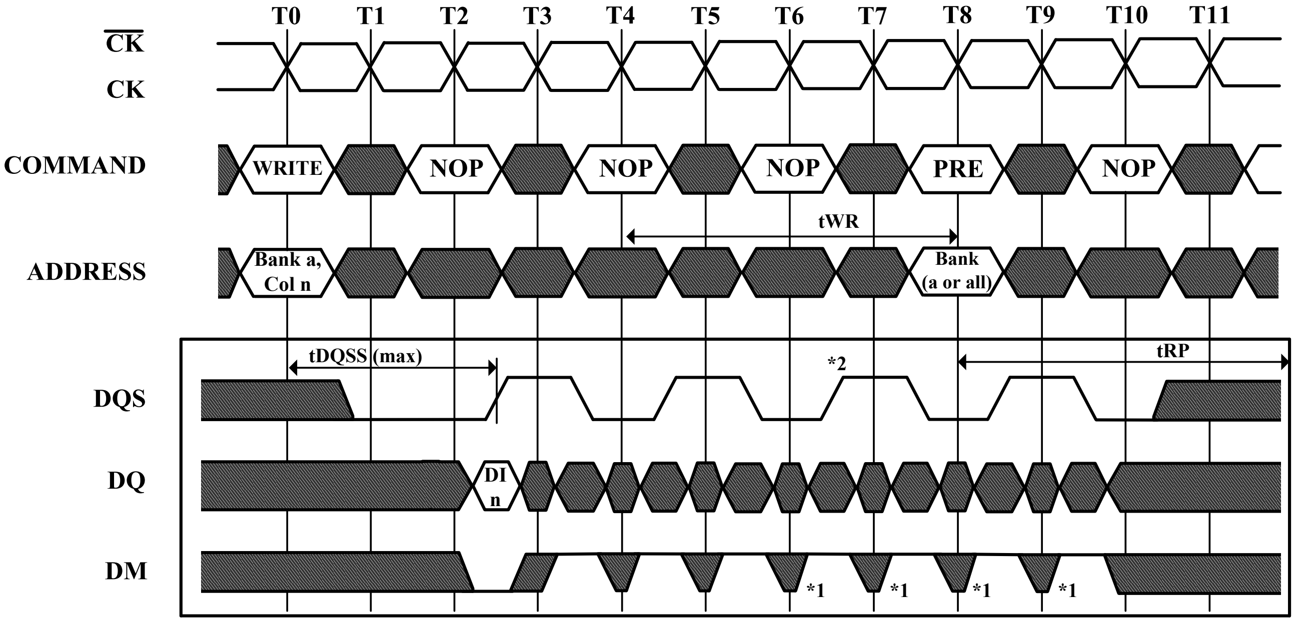
*1 = can be don't care for programmed burst length of 4

*2 = for programmed burst length of 4, DQS becomes don't care at this point

DM= UDM & LDM

Don't Care

Figure 42. Write to Precharge Max tDQSS ODD Number of Data Interrupting



DI n = Data In for column n
An interrupted burst of 4 or 8 is shown, 1 data element is written
tWR is referenced from the first positive CK edge after the last Data In Pair
A10 is LOW with the WRITE command (AUTO PRECHARGE is disabled)
*1 = can be don't care for programmed burst length of 4
*2 = for programmed burst length of 4, DQS becomes don't care at this point
DM= UDM & LDM

Don't Care

Figure 43. Precharge Command

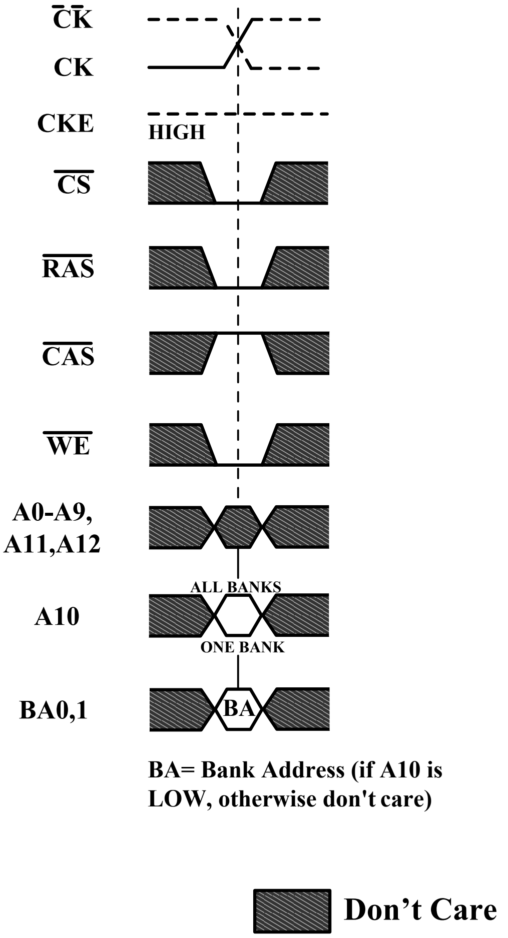


Figure 44. Power-Down

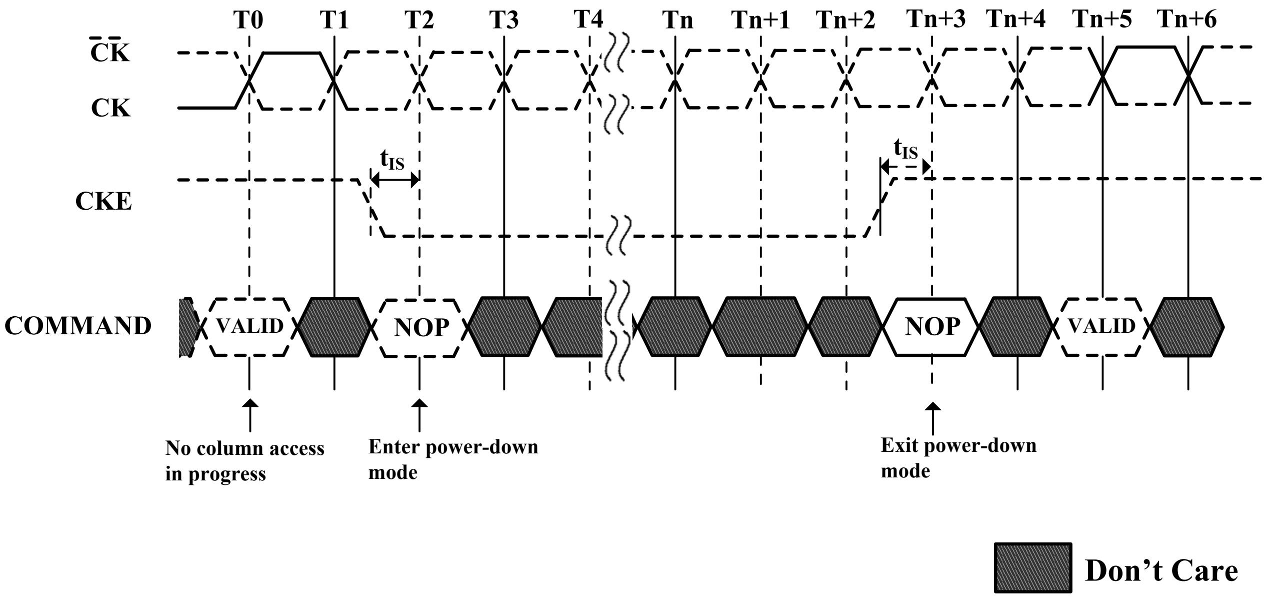


Figure 45. Clock Frequency Change in Precharge

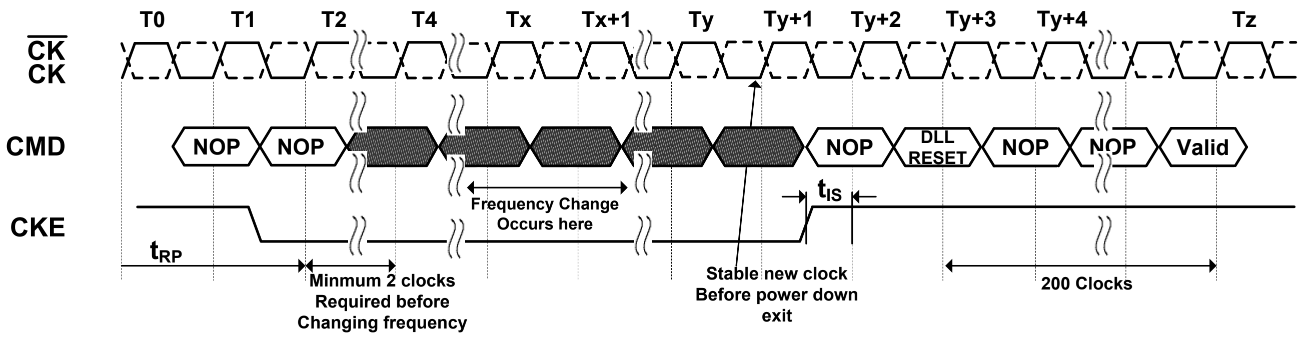
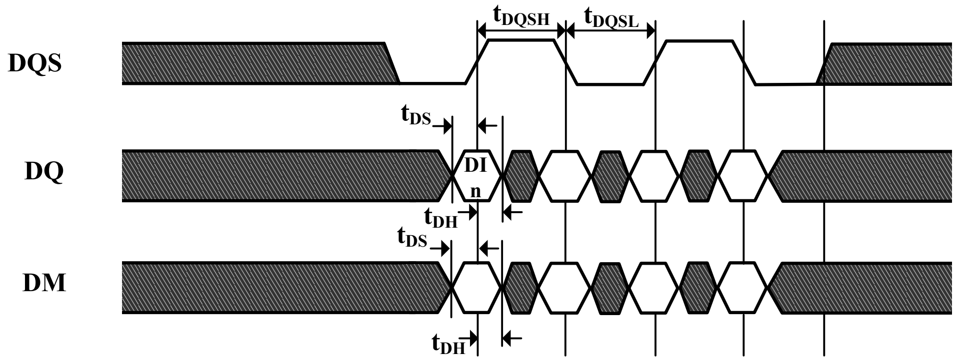


Figure 46. Data input (Write) Timing



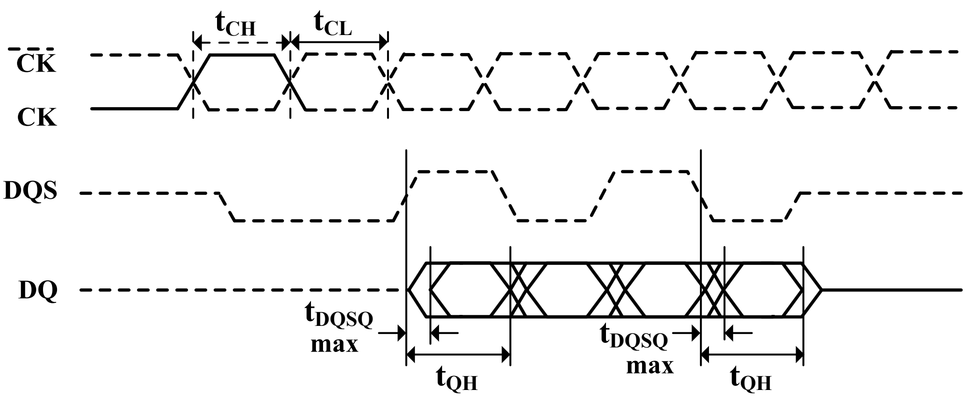
DI n = Data In for column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are applied in the programmed order following DI n

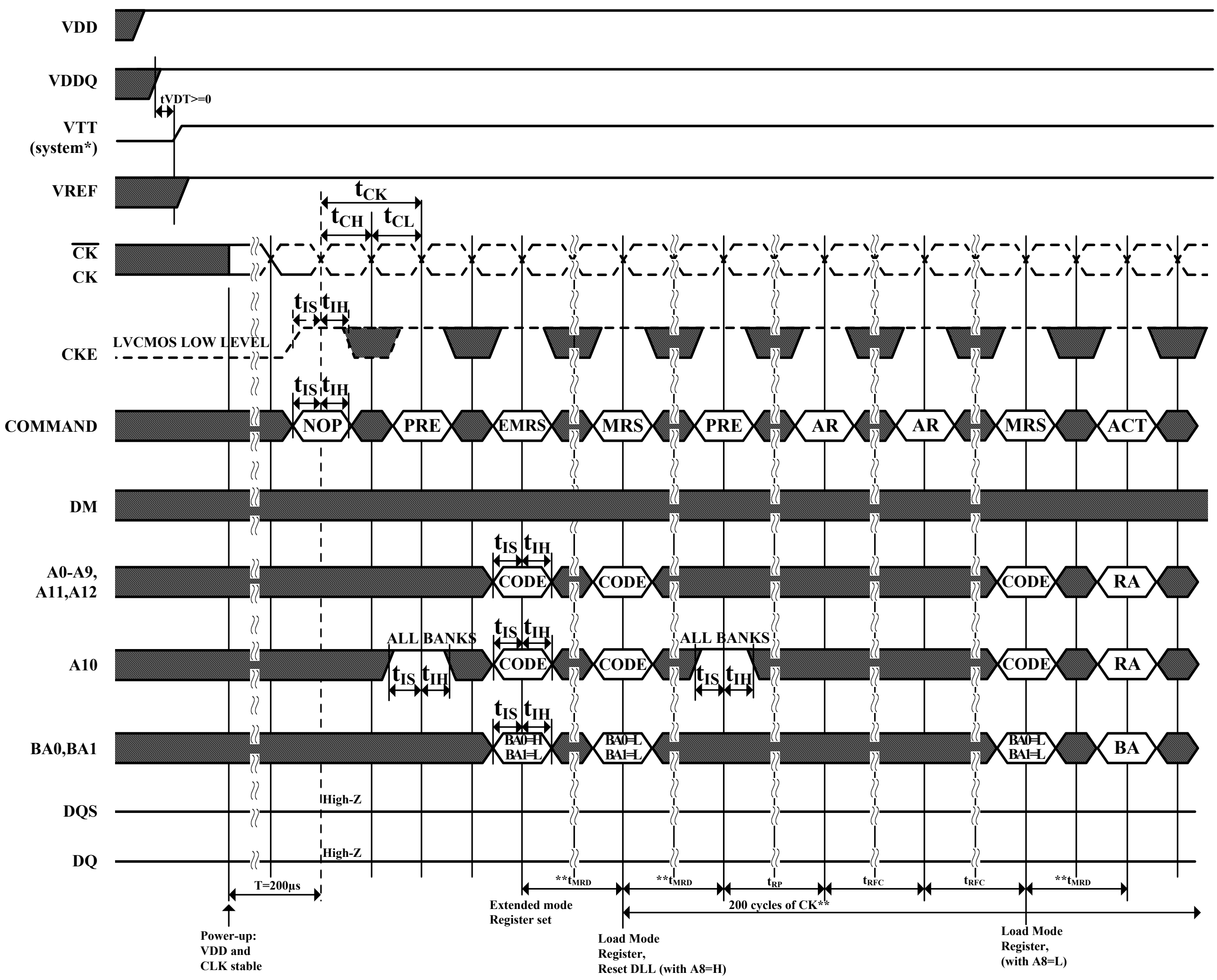
Don't Care

Figure 47. Data Output (Read) Timing



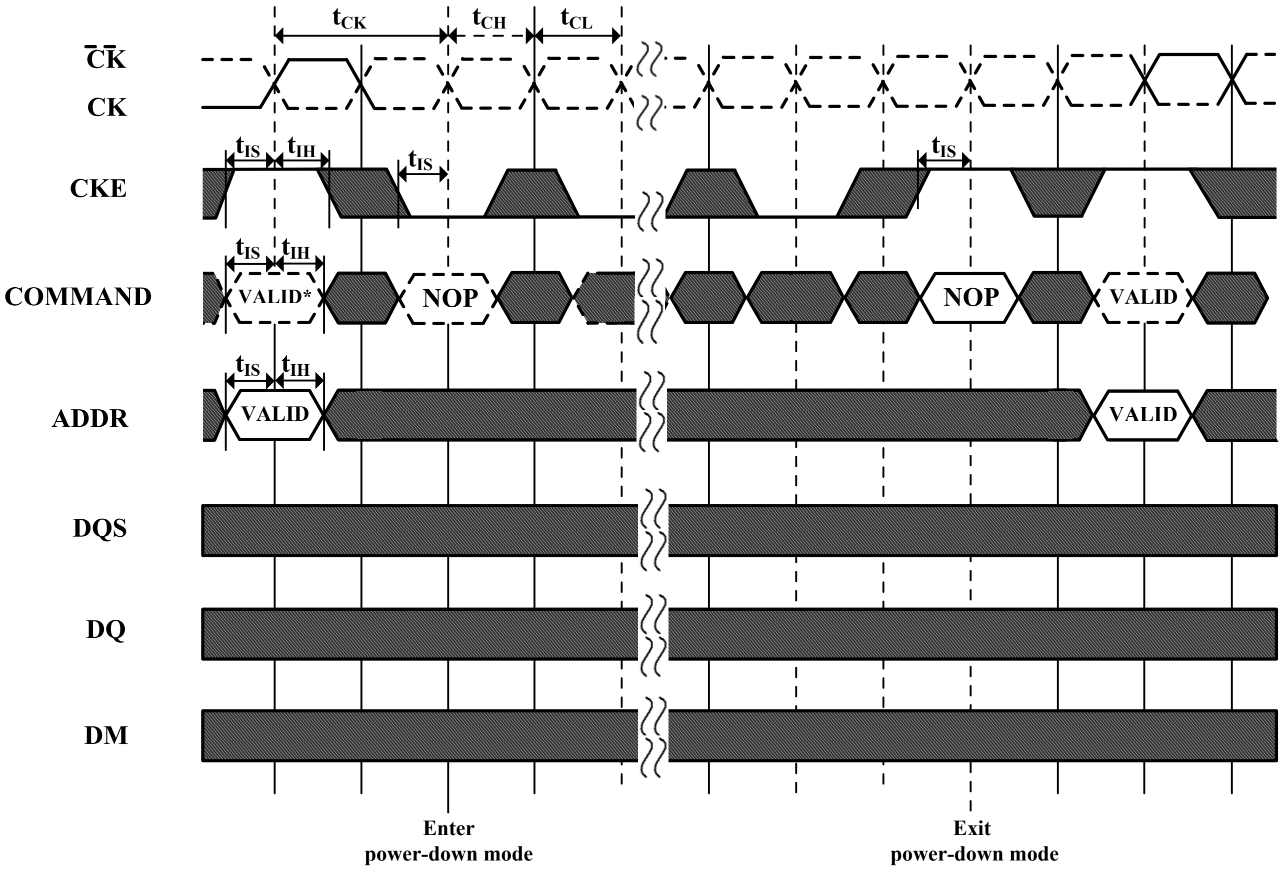
Burst Length = 4 in the case shown

Figure 48. Initialize and Mode Register Sets



***=VTT is not applied directly to the device, however tVTD must be greater than or equal to zero to avoid device latch-up.**
**** = tMRD is required before any command can be applied, and 200 cycles of CK are required before any executable command can be applied the two auto Refresh commands may be moved to follow the first MRS but precede the second PRECHARGE ALL command.**

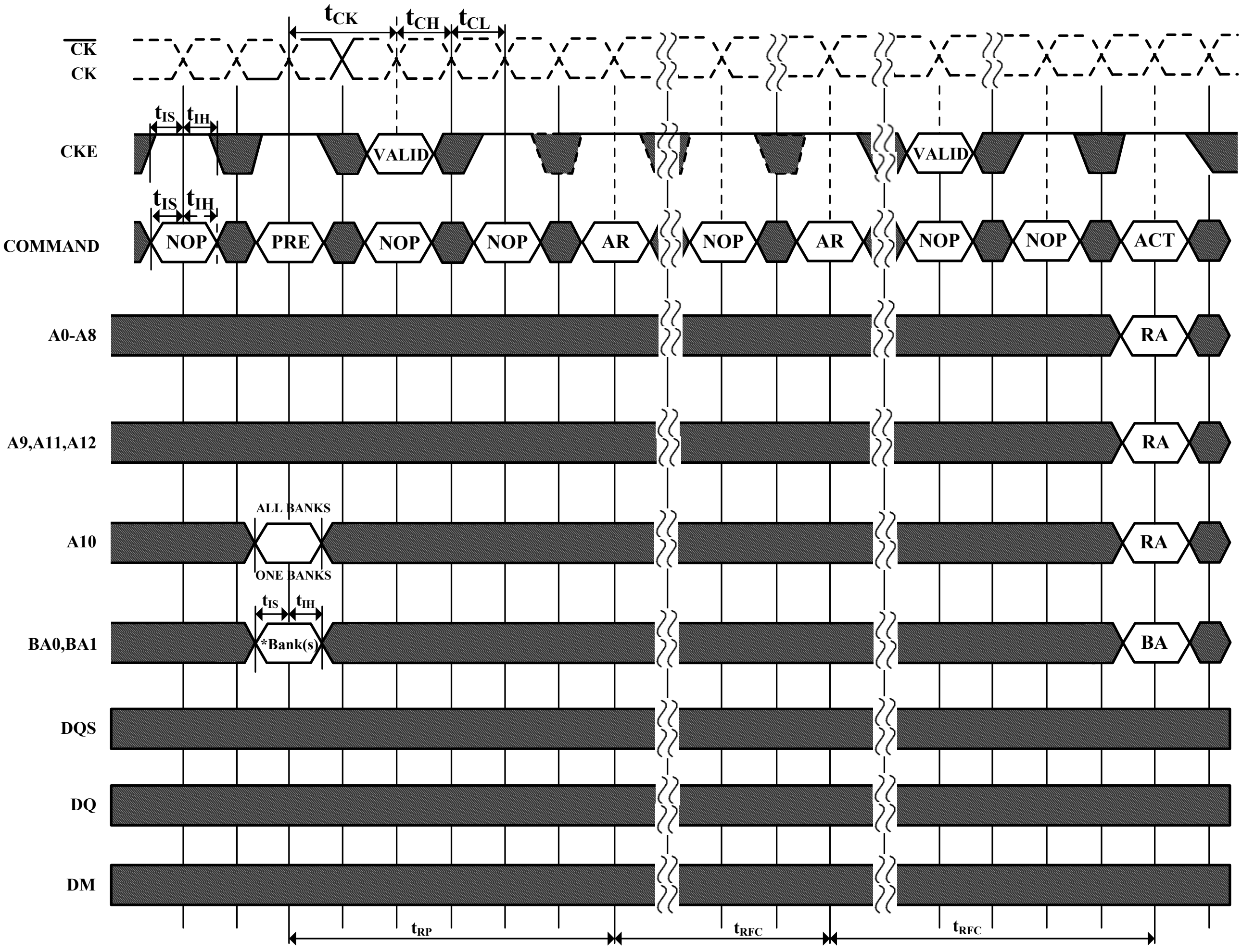
Figure 49. Power Down Mode



No column accesses are allowed to be in progress at the time Power-Down is entered
*=If this command is a PRECHARGE ALL (or if the device is already in the idle state) then the Power-Down mode shown is Precharge Power Down. If this command is an ACTIVE (or if at least one row is already active) then the Power-Down mode shown is active Power Down.

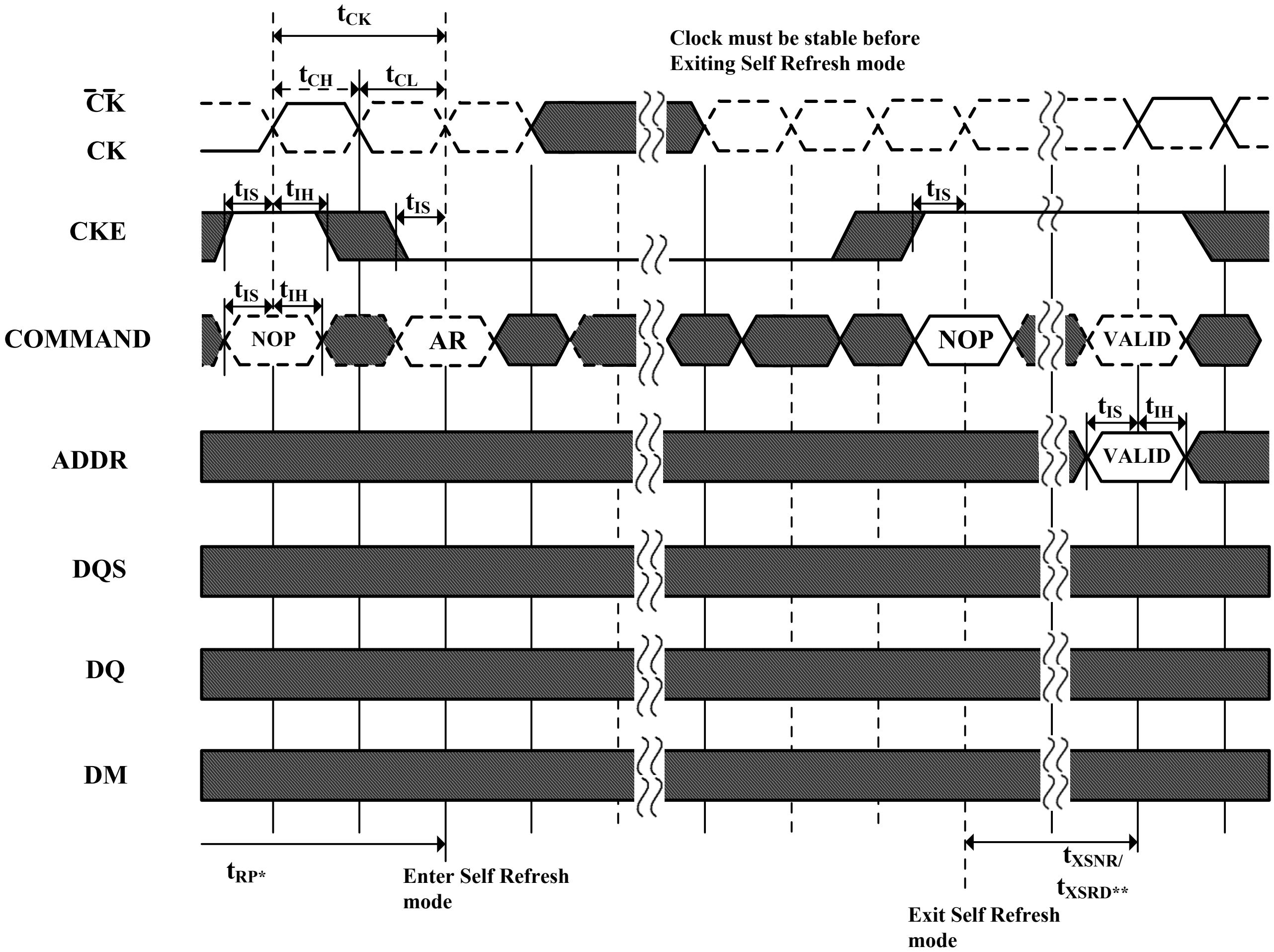
Don't Care

Figure 50. Auto Refresh Mode



* = "Don't Care", if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks)
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH
NOP commands are shown for ease of illustration; other valid commands may be possible after tRFC
DM, DQ and DQS signals are all "Don't Care"/High-Z for operations shown

Figure 51. Self Refresh Mode

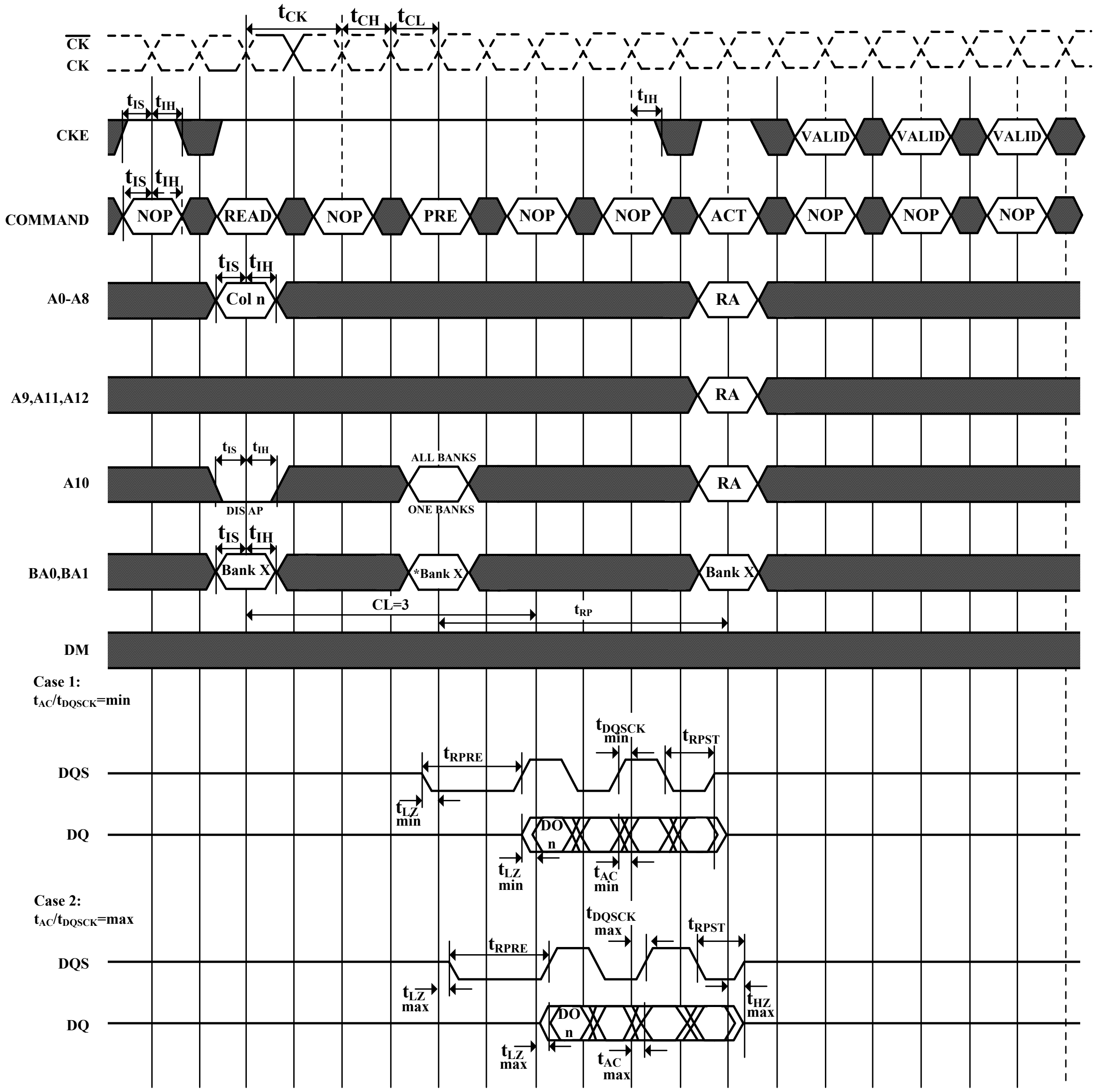


* = Device must be in the "All banks idle" state prior to entering Self Refresh mode

** = tXSNR is required before any non-READ command can be applied, and tXSRD (200 cycles of CK) is required before a READ command can be applied.

Don't Care

Figure 52. Read without Auto Precharge



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

* = “Don't Care”, if A10 is HIGH at this point

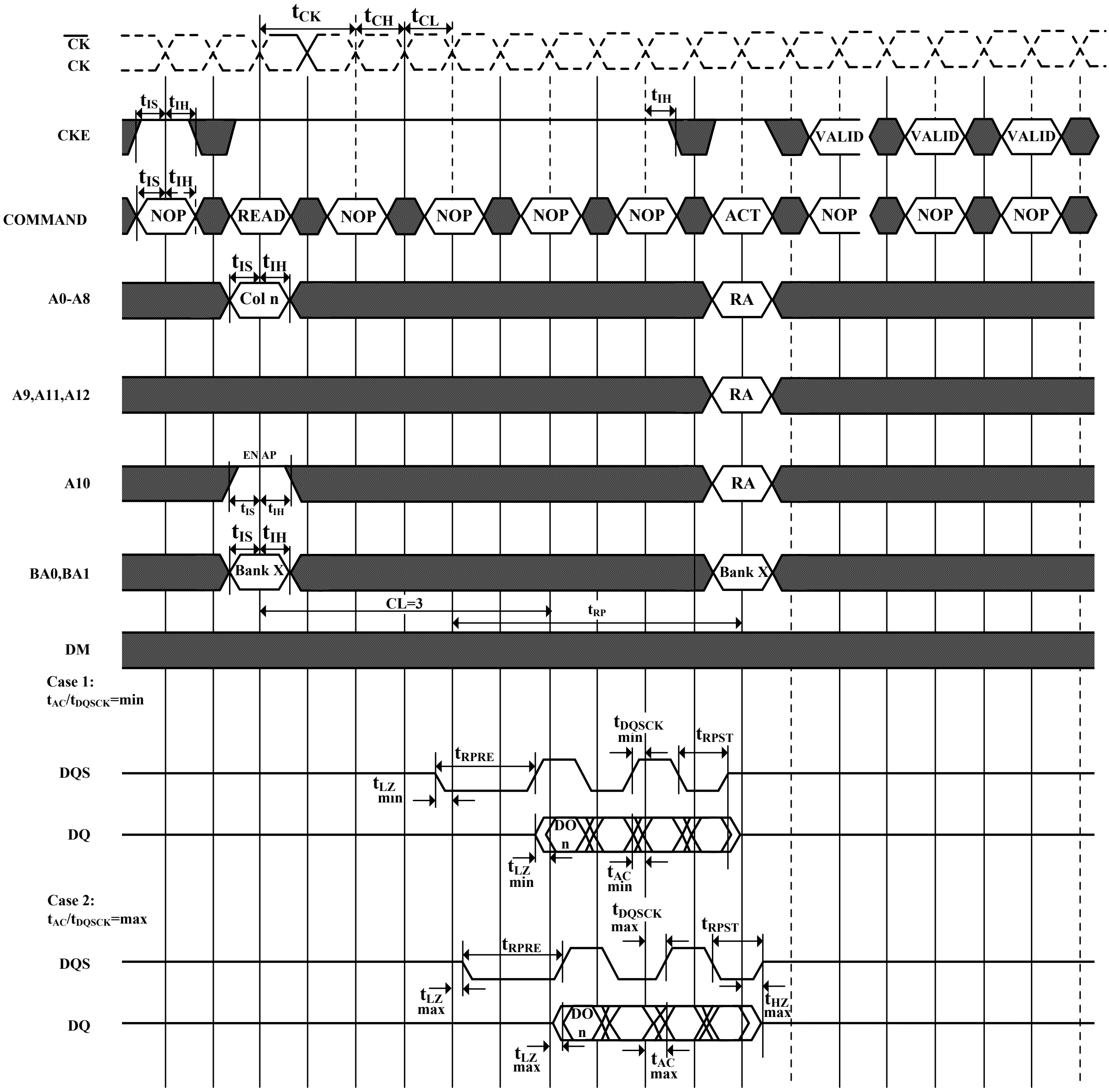
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

NOP commands are shown for ease of illustration; other commands may be valid at these times

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don’t Care

Figure 53. Read with Auto Precharge



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

EN AP = Enable Autoprecharge

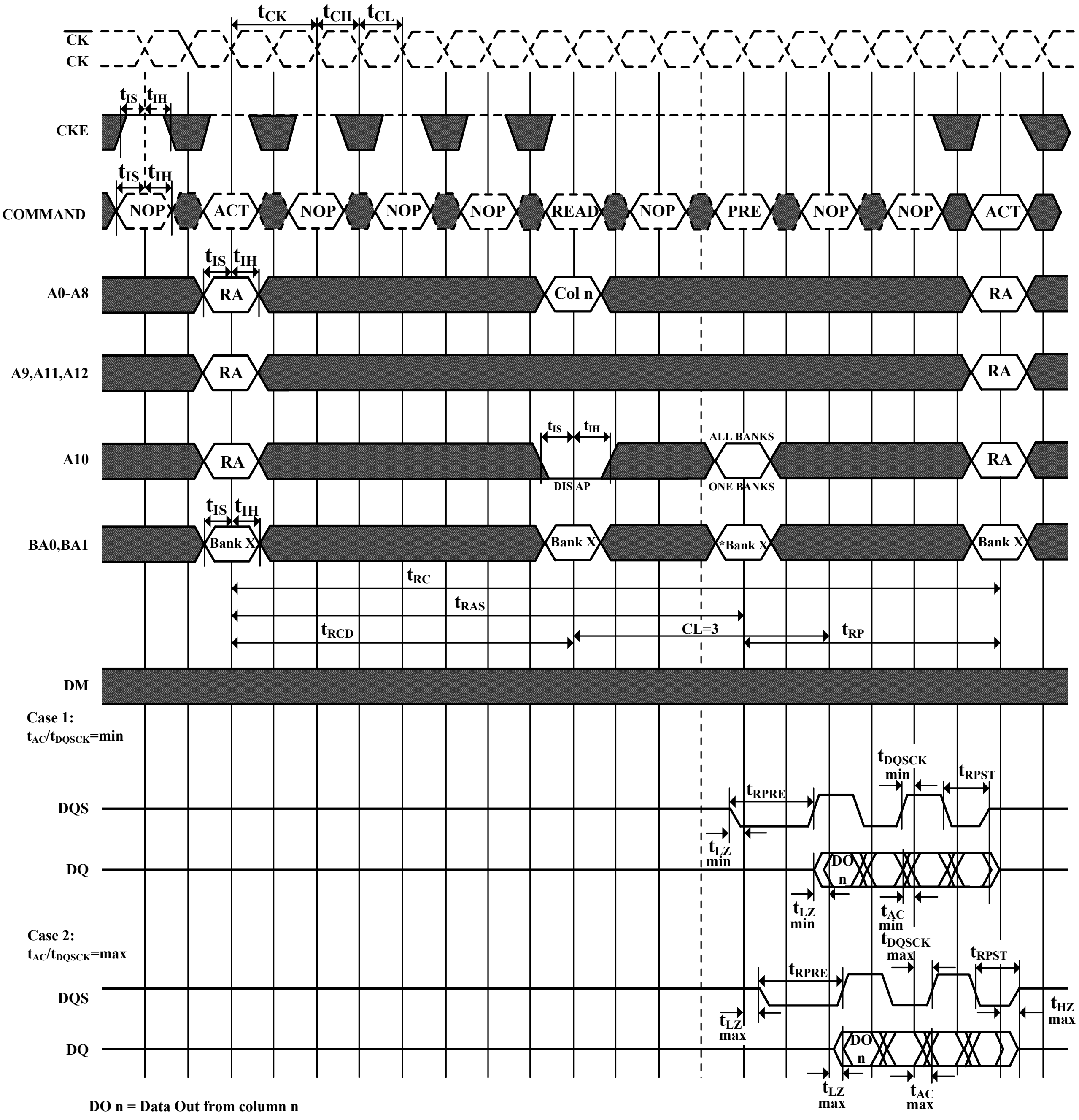
ACT = ACTIVE, RA = Row Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

The READ command may not be issued until tRAP has been satisfied. If Fast Autoprecharge is supported, tRAP = tRCD, else the READ may not be issued prior to tRASmin - (BL*tCK/2)

Don't Care

Figure 54. Bank Read Access



DO n = Data Out from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DO n

DIS AP = Disable Autoprecharge

* = " Don't Care" , if A10 is HIGH at this point

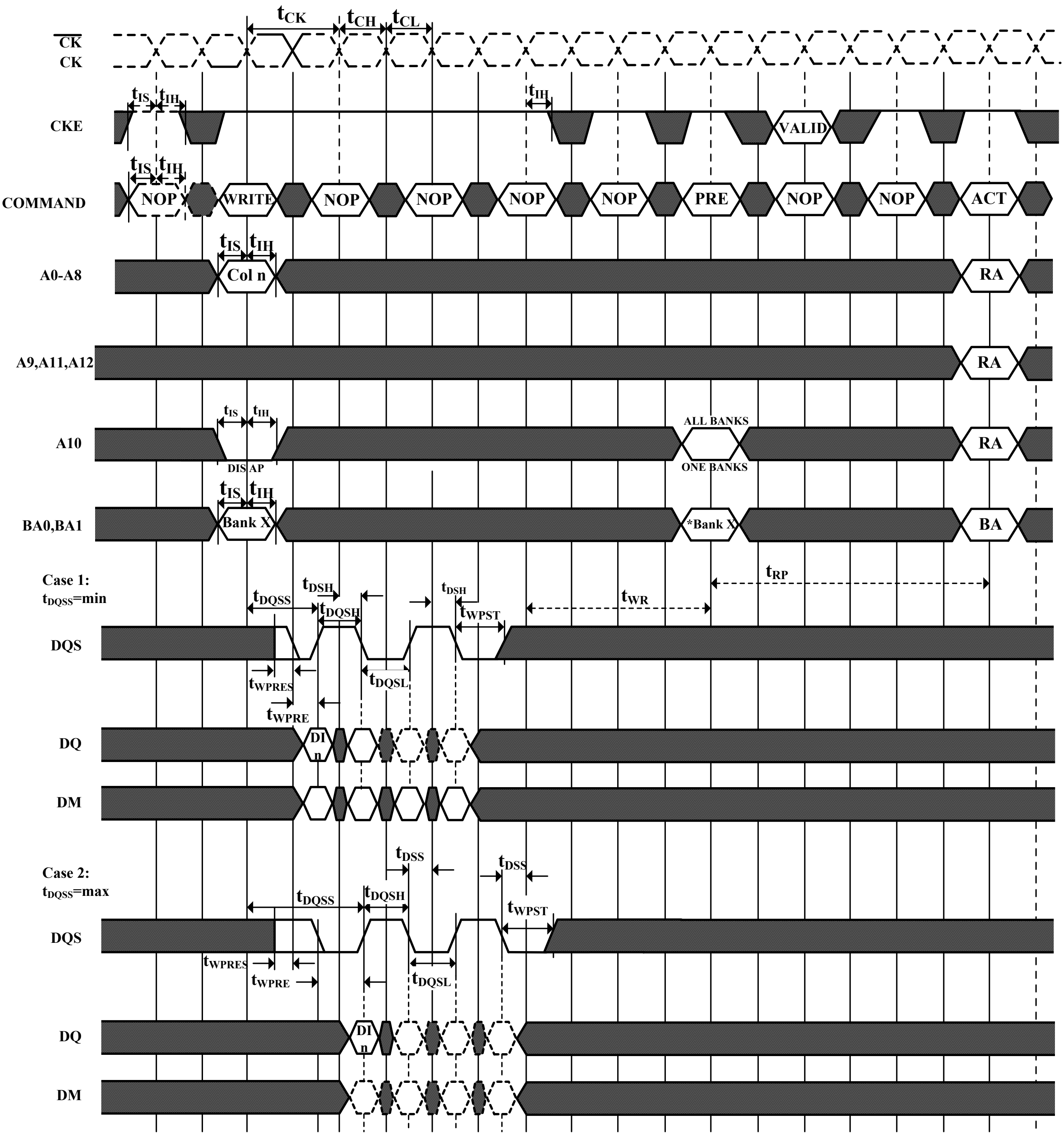
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Note that tRCD > tRCD MIN so that the same timing applies if Autoprecharge is enabled (in which case tRAS would be limiting)

Don't Care

Figure 55. Write without Auto Precharge



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care", if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address, AR = AUTOREFRESH

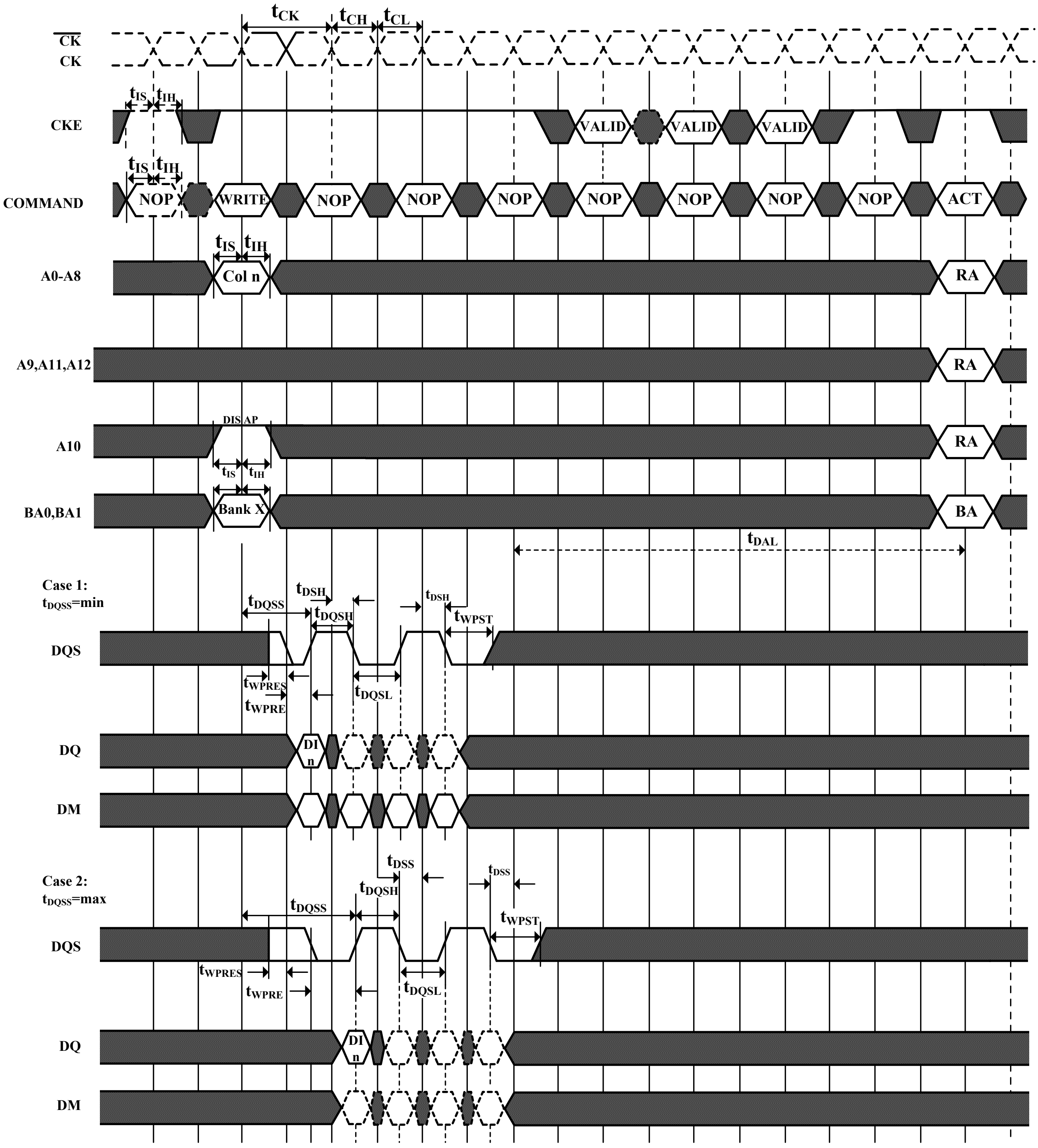
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care

Figure 56. Write with Auto Precharge



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

EN AP = Enable Autoprecharge

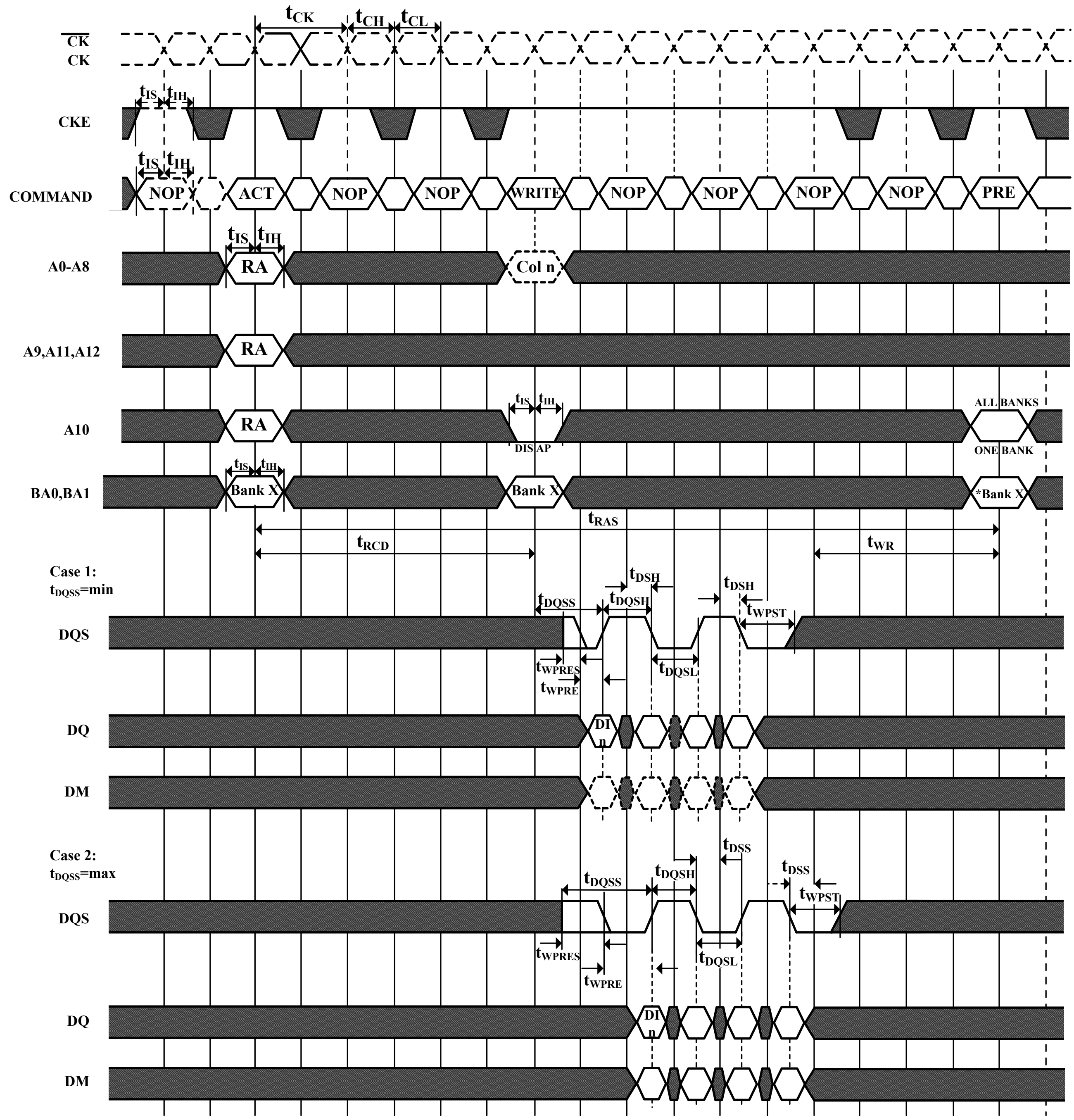
ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Don't Care

Figure 57. Bank Write Access



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data Out are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care" , if A10 is HIGH at this point

PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

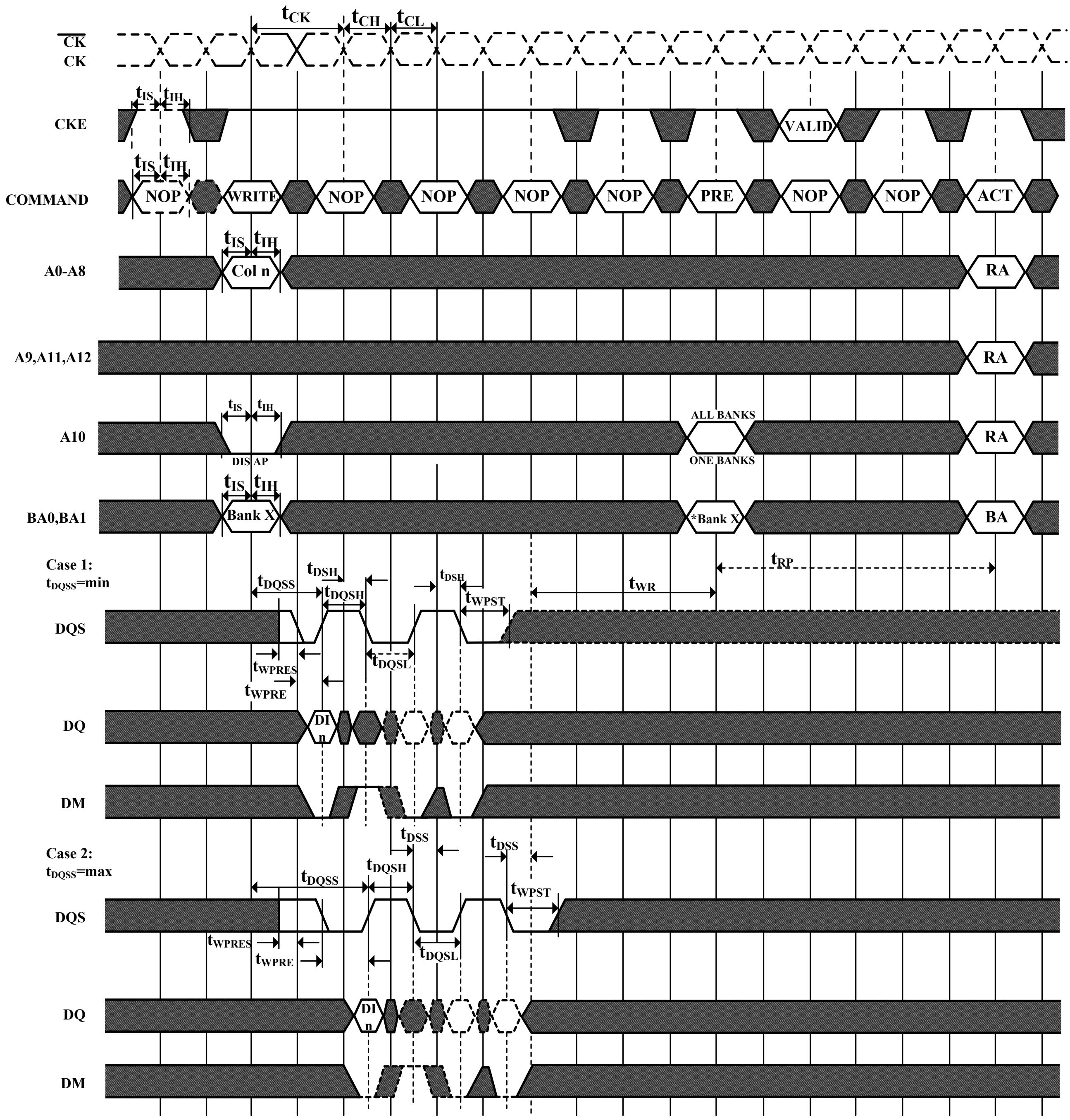
NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Don't Care

Figure 58. Write DM Operation



DI n = Data In from column n

Burst Length = 4 in the case shown

3 subsequent elements of Data In are provided in the programmed order following DI n

DIS AP = Disable Autoprecharge

*=" Don't Care", if A10 is HIGH at this point

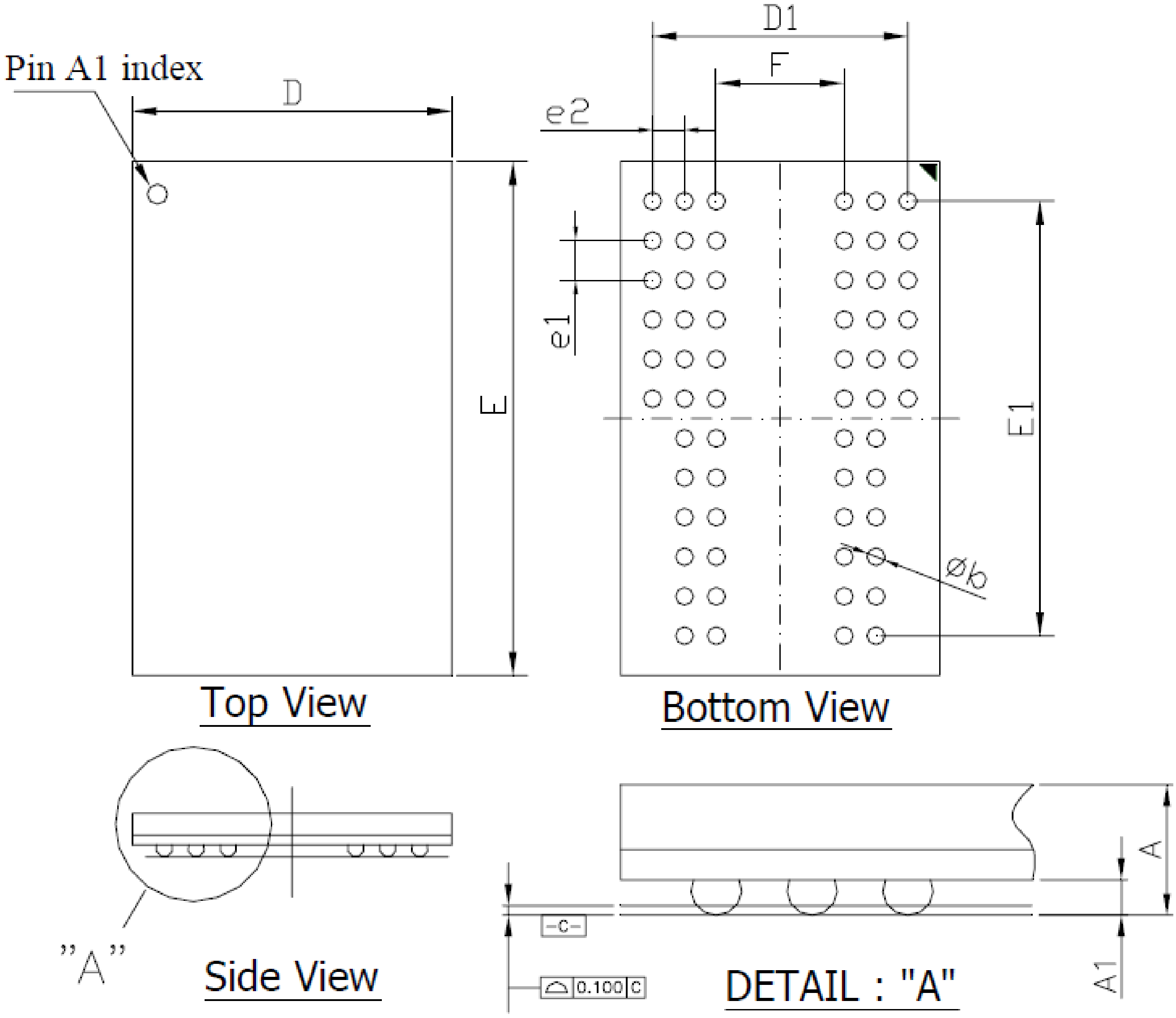
PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address

NOP commands are shown for ease of illustration; other commands may be valid at these times

Although tDQSS is drawn only for the first DQS rising edge, each rising edge of DQS must fall within the ± 25% window of the corresponding positive clock edge

Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks

Figure 59. 60ball FBGA Package 8x13x1.2 mm(max) Outline Drawing Information



Symbol	Dimension (inch)			Dimension (mm)		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.047	--	--	1.20
A1	0.012	0.014	0.016	0.30	0.35	0.40
D	0.311	0.315	0.319	7.90	8.00	8.10
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.433	--	--	11.00	--
e1	--	0.039	--	--	1.00	--
e2	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
F	--	0.126	--	--	3.20	--

PART NUMBERING SYSTEM

AS4C	16M16D1	-5	B	A	N	XX
DRAM	16M16 =16M x 16 D1=DDR1	5=200MHz	B=FBGA	A=Automotive temp -40°C~ 105°C	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel

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