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## 1. Information

<b>Product</b>	2Gb DDR3 SDRAM
<b>Device</b>	AS4C128M16D3B-12BCN
<b>Technology</b>	30nm
<b>Function</b>	128M*16 DDR3

<b>Package Type</b>	96B FBGA
<b>Substrate</b>	BT
<b>Solder Ball</b>	Sn-Ag-Cu solder ball
<b>Molding Compound</b>	HITACHI CEL-9120HF
<b>Package Size</b>	8*13 mm <sup>2</sup>

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## 2. Life Test

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
2.1 High Temperature Operation Life Test *	Ta = 125 °C ; array VDD =1.5V	515	168hrs 500hrs 1000hrs	0/515 0/515 0/515
2.2 Low Temperature Operation Life Test *	Ta = -40 °C ; array VDD =1.5V	105	168hrs 500hrs 1000hrs	0/105 0/105 0/105

Remark:

\* Preconditioning:

Baking @ 125°C , 24 hours. => Soaking @ 30°C / 60% R.H., 192 hours => IR : 3 times.

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
2.3 Early Failure Rate	Ta = 125 °C ; array VDD = 1.5V	5,685	24hrs	1/5685

\* SCF (Single cell fail) \*1

Root Cause: Capacitor - Capacitor short issue

Corrective Action: New container oxide Etch recipe to open process window for capacitor-capacitor short issue improvement.

### 3. Environmental Test

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
3.1 High Temperature Storage Life Test *	Ta. = 150°C	231	168hrs 500hrs 1000hrs	0/231 0/231 0/231
3.2 Temperature Cycle Test *	Ta.= -55°C / +125°C, 2 cys/ Hr	231	500cycs 1000cycs	0/231 0/231
3.3 Highly Accelerated Stress Test *	Ta. = 130°C/ 85%RH;	231	144hrs	0/231

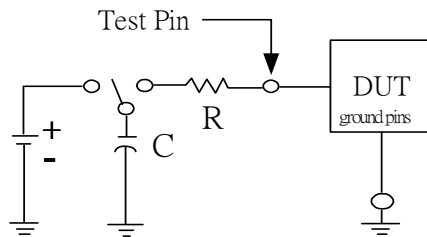
Remark:

\*. Preconditioning

Baking @ 125°C , 24 hours. => Soaking @ 30°C / 60% R.H., 192 hours => IR : 3 times.

## 4. ESD Sensitivity

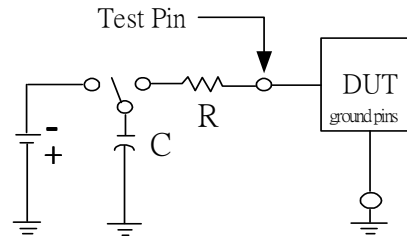
4.1 a. Human Body Model (HBM) Test Circuit



\* Human Body Model (HBM)

- Stress Voltage :  $> \pm 4000V$

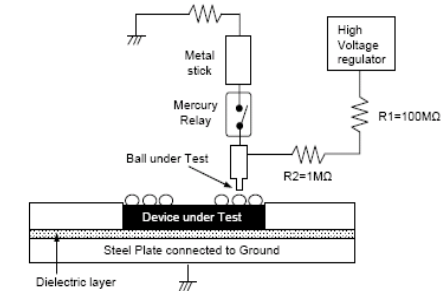
b. Machine Mode (MM) test circuit:



\* Machine Model (MM)

- Stress Voltage :  $\pm 300V$

c. Charge Device Model (CDM) test circuit



Charge Device Model (CDM)

- Stress Voltage :  $> \pm 750V$

4.2 Reference: HBM: JESD22-A114-B; MM: JESD22-A115-E; CDM: ANSI/ ESD SP 5.3.2

4.3 Sample size : 3 ea/ lot, total 3 lots

4.4 Judgment Criteria : Pass Leakage, standby current and functionality tests at both high and low temperature.

4.3 Test Result : **HBM :  $> \pm 4000V$**

**MM :  $> \pm 300V$**

**CDM :  $> \pm 750V$**



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## 5. Latch-up Test

Test Items	Test Conditions	Sample Size	Results (Number of failures)
5.1 I-test (Positive and Negative)	$>\pm 150\text{mA}$	6 ea/ lot, total 3 lots	0/18
5.2 V-supply over voltage test	$>\pm 1.5 \text{ max. } V_{\text{supply}}$	6 ea/ lot, total 3 lots	0/18

5.3 Reference: Test procedure in according to EIA/JESD 78A

5.4 Judgment Criteria : Pass Leakage, standby current and functionality tests at both high and low temperature.

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