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## 2. Life Test

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
2.1 High Temperature Operation Life Test *	Ta = 125 °C; VDD =1.5V	231	168hrs	0/231
			500hrs	0/231
			1000Hrs	0/231
2.2 Low Temperature Operation Life Test *	Ta = -10 °C; VDD =1.5V	77	168hrs	0/77
			500hrs	0/77
			1000Hrs	0/77

Remark:

\*. Preconditioning

- 1) Temp. Cycling (-65C/+150C) 20 cycles
- 2) High temp. storage 125°C baking = 10h
- 3) 30C/ 60%RH 192h moisture soak (JEDEC level3)
- 4) Reflow. 3time (J-STD-020)

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
2.3 Early Life Failure Rate	Ta = 110 °C; VDD = 1.6V	10,000	24hrs	0/10000

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### 3. Environmental Test

Test Items	Test Conditions	Sample Size	Stress Hours	Results (Number of failures)
3.1 High Temperature Storage Life Test *	Ta. = 150°C	77	168hrs 500hrs 1000hrs	0/77 0/77 0/77
3.2 Temperature Cycle Test *	Ta.= -65°C / +150°C	231	200 cycs 500cycs 1000cycs	0/231 0/231 0/231
3.3 Highly Accelerated Temperature and Humidity Stress	Ta. = 110°C/ 85%RH; VDD = 1.6V	231	168hrs 264hrs	0/231 0/231

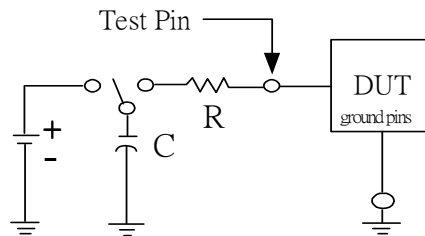
Remark:

\*. Preconditioning

- 1) Temp. Cycling (-65C/+150C) 20 cycles
  - 2) High temp. storage 125°C baking = 10h
  - 3) 30C/ 60%RH 192h moisture soak (JEDEC level3)
  - 4) Reflow. 3time (J-STD-020)
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## 4. ESD Sensitivity

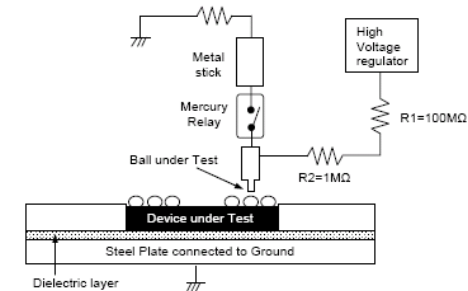
### 4.1 Human Body Model (HBM) Test Circuit



#### \* Human Body Model (HBM)

- Capacitance : 100 pF, Resistance : 1.5 KΩ  
3 pulses per polarity  
1 sec interval between pluses
- Sample size : 3ea
- Stress Voltage : >±2000V

### 4.2 Charge Device Model (CDM) test circuit:



- Direct charging method  
3 pulses per polarity  
1 sec interval between pluses
- Sample size : 3 ea
- Stress Voltage : >±1000V (Corner Balls)  
> ±500V (All other Balls)

4.2 Reference: HBM: MIL-STD-883 Method 3015.8-2012; CDM: ESD S5.3.1-2009

4.3 Test Result : **HBM : > 2000V; CDM : > 1000V (Corner Balls)**  
**> 500V (All other Balls)**

## 5. Latch-up Test

Test Items	Test Conditions	Sample Size	Results (Number of failures)
5.1 I-test (I/O pin current pulse injection)	$>\pm 200\text{mA}$ ; $T_c = 95\text{ }^\circ\text{C}$	6 ea	0/6
5.2 V-supply over voltage test	$>\pm 2.36\text{V}$ ; $T_c = 95\text{ }^\circ\text{C}$	6 ea	0/6

5.2 Reference: Test procedure in according to EIA/JESD 78, test temp. is Class2 and failure criteria is Level A.

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