32Gb (4G x 8) Dual Die DDR4 SDRAM

AS4C4G8D4 - 128 Meg x 8 x 16 Banks x 2 Ranks

Revision History

Revision	Details	Date
Rev 1.0	Initial Release	Sept. 2024

Description

The 32Gb (Dual Die) DDR4 SDRAM uses 16Gb DDR4 SDRAM die (essentially two ranks of the 16Gb DDR4 SDRAM). Refer to Alliance's 16Gb DDR4 SDRAM data sheet for the specifications not included in this document.

Features

- Uses 16Gb die
- Two ranks (includes dual CS#, ODT, and CKE balls)
- Each rank has 4 groups of 4 internal banks for concurrent operation
- $V_{DD} = V_{DDQ}$ = 1.2V (1.14–1.26V)
- 1.2V V_{DDQ}-terminated I/O
- JEDEC-standard ball-out
- Low-profile package
- T_C of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

Options / Marking

Options	Marking
• Configuration	
– 128 Meg x 8 x 16 banks x 2 ranks	4G8
• FBGA package (Pb-free)	
– 78-ball FBGA (7.5mm x 11mm x 1.2mm)	
• Timing – cycle time	
– 0.625ns @ CL = 22 (DDR4-3200)	-62
• Self refresh	None
– Standard	
• Operating temperature	
– Commercial (0°C ≤ TC ≤ 95°C)	None

Table 1: Key Timing Parameters

Speed Grade[1]	Data Rate (MT/s)	Target CL-*n*RCD-*n*RP	^tAA (ns)	^tRCD (ns)	^tRP (ns)
-62	3200	22-22-22	13.75	13.75	13.75

Notes: 1. Refer to the Speed Bin Tables for additional details.

Table 2: Ordering Information

Product part No	Org	Temperature Tc	Max Clock (MHz)	Package
AS4C4G8D4-62BCN	**4G x 8**	**Commercial 0°C to 95°C**	**1600**	**78-ball FBGA 7.5x11mm**

Table 3: Addressing

Parameter	4096 Meg x 8
Configuration	128 Meg x 8 x 16 banks x 2 ranks
Bank group address	BG[1:0]
Bank count per group	4
Bank address in bank group	BA[1:0]
Row address	128K A[16:0]
Column address	1K A[9:0]

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Functional Description

The Dual Die DDR4 SDRAM is a high-speed, CMOS dynamic random access memory device internally configured as two 16-bank DDR4 SDRAM devices.

Although each die is tested individually within the dual-die package, some Dual Die test results may vary from a like-die tested within a monolithic die package.

The DDR4 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR4 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR4 SDRAM and edge-aligned to the data strobes.

Read and write accesses to the DDR4 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Operation begins with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

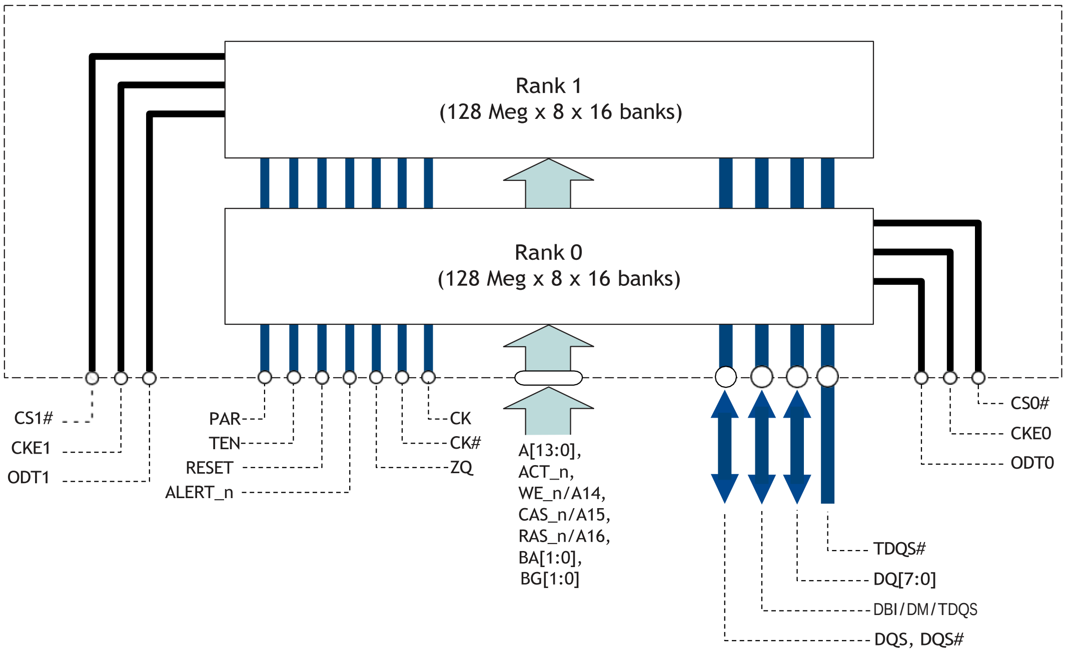
This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Alliance monolithic DDR4 data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Commercial Temperature

The industrial temperature (IT) option, if offered, requires that the case temperature not exceed 0°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance, I_{DD} values, some I_{DD} specifications and the input/output impedance must be derated when T_C is < 0°C or > 95°C. See the DDR4 monolithic data sheet for details.

Functional Block Diagrams

Figure 1: Functional Block Diagram (128 Meg x 8 x 16 Banks x 2 Ranks)



Electrical Specifications - Leakages

Table 4: Input and Output Leakages

Symbol	Parameter	Min	Max	Units	Notes
I_{IN}	Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.1V (All other pins not under test = 0V)	-4	4	µA	1
I_{VREFCA}	V_{REF} supply leakage current (All other pins not under test = 0V)	-4	4	µA	2
I_{ZQ}	Input leakage on ZQ pin	-100	20	µA	
I_{TEN}	Input leakage on TEN pin	-12	20	µA	
I_{OZpd}	Output leakage: V_{OUT} = V_{DDQ}	–	20	µA	3
I_{OZpu}	Output leakage: V_{OUT} = V_{SSQ}	-100	–	µA	3, 4

Notes: 1. Any input 0V < V_{IN} < 1.1V
2. V_{REFCA} = V_{DD}/2, V_{DD} at valid level.
3. DQ are disabled.
4. ODT is disabled with the ODT input HIGH.

Temperature and Thermal Impedance

It is imperative that the DDR4 SDRAM device's temperature specifications, shown in the following table, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances listed in apply to the current die revision and packages.

Incorrectly using thermal impedances can produce significant errors. Read Alliance technical note , "Thermal Applications," prior to using the values listed in the thermal impedance table. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the die size reduction.

The DDR4 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table **5**: Thermal Characteristics

Parameter	Symbol	Value	Units	Notes
Operating temperature	T_C	0 to 85	°C	
		0 to 95	°C	4

Notes: 1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of self refresh temperature (SRT) or automatic self refresh (ASR), if available, must be enabled.
5. Notes 1-3 apply to entire table.

Figure 2: Temperature Test Point Location

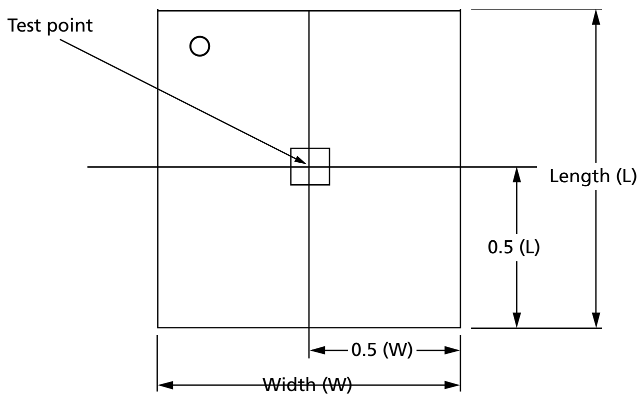


Table **6**: Thermal Impedance

Package	Substrate	Θ JA (°C/W) Airflow = 0m/s	Θ JA (°C/W) Airflow = 1m/s	Θ JA (°C/W) Airflow = 2m/s	Θ JB (°C/W)	Θ JC (°C/W)	Notes
78-ball	Low conductivity	51.2	39.1	34.5	NA	2.6	1
	High conductivity	30.2	25.0	23.3	10.4	NA	

Notes: 1. Thermal resistance data is based on a typical number.

Electrical Characteristics - AC and DC Output Measurement Levels

Single-Ended Outputs

Table 7: Single-Ended Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
DC output high measurement level (for IV curve linearity)	$V_{OH(DC)}$	$1.1 \times V_{DDQ}$	V
DC output mid measurement level (for IV curve linearity)	$V_{OM(DC)}$	$0.8 \times V_{DDQ}$	V
DC output low measurement level (for IV curve linearity)	$V_{OL(DC)}$	$0.5 \times V_{DDQ}$	V
AC output high measurement level (for output slew rate)	$V_{OH(AC)}$	$(0.7 + 0.15) \times V_{DDQ}$	V
AC output low measurement level (for output slew rate)	$V_{OL(AC)}$	$(0.7 - 0.15) \times V_{DDQ}$	V

Notes: 1. The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals.

Table **8**: Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TR_{se}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]/\Delta TF_{se}$

Figure 3: Single-Ended Output Slew Rate Definition

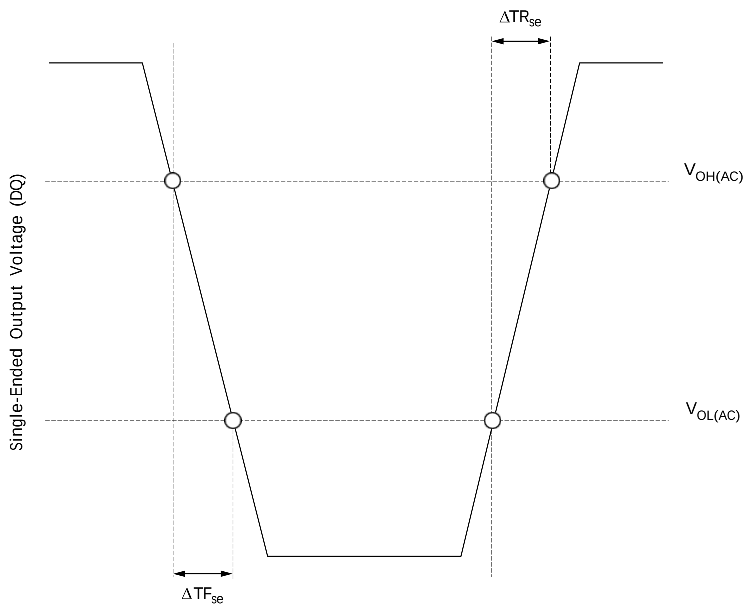


Table **9**: Single-Ended Output Slew Rate

Parameter	Symbol	DDR4-1333 to DDR4-3200		Unit
		Min	Max	
Single-ended output slew rate	SRQ_{se}	2	7	V/ns

Notes: 1. For $R_{ON} = R_{ZQ}/7$.
2. SR = slew rate; Q = query output; se = single-ended signals.
3. In two cases a maximum slew rate of 12V/ns applies for a single DQ signal within a byte lane:
   - Case 1 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are static (they stay at either HIGH or LOW).
   - Case 2 is defined for a single DQ signal within a byte lane that is switching into a certain direction (either from HIGH-to-LOW or LOW-to-HIGH) while all remaining DQ signals in the same byte lane are switching into the opposite direction (from LOW-to-HIGH or HIGH-to-LOW, respectively). For the remaining DQ signal switching into the opposite direction, the standard maximum limit of 7 V/ns applies.

Differential Outputs

Table 10: Differential Output Levels

Parameter	Symbol	DDR4-1600 to DDR4-3200	Unit
AC differential output high measurement level (for output slew rate)	$V_{OH,diff(AC)}$	$0.3 \times V_{DDQ}$	V
AC differential output low measurement level (for output slew rate)	$V_{OL,diff(AC)}$	$-0.3 \times V_{DDQ}$	V

Notes: 1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7 and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each differential output.

Using the same reference load used for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL,diff(AC)}$ and $V_{OH,diff(AC)}$ for differential signals.

Table 11: Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OL,diff(AC)}$	$V_{OH,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OH,diff(AC)}$	$V_{OL,diff(AC)}$	$[V_{OH,diff(AC)} - V_{OL,diff(AC)}]/\Delta TF_{diff}$

Figure 4: Differential Output Slew Rate Definition

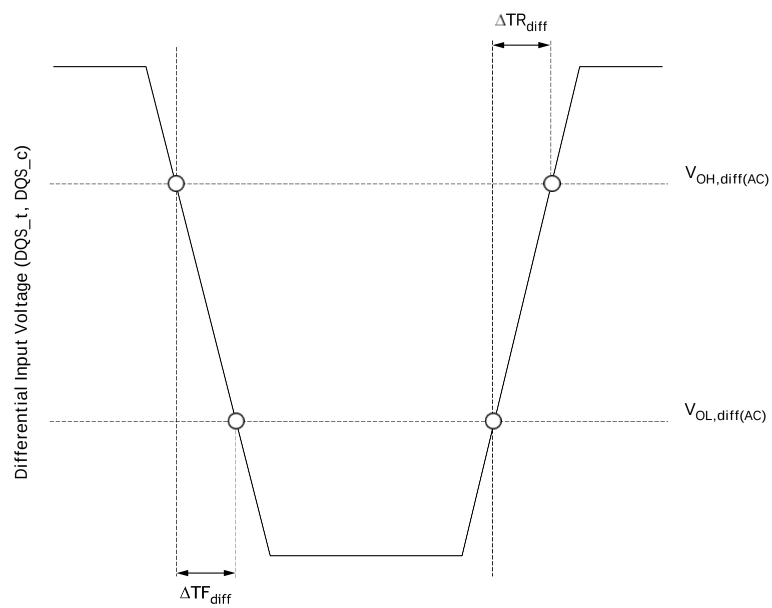


Table 12: Differential Output Slew Rate

Parameter	Symbol	DDR4-1333 to DDR4-3200		Unit
		Min	Max	
Differential output slew rate	SRQ_{diff}	8	18	V/ns

Notes: 1. For $R_{ON} = R_{ZQ}/7$.
2. SR = slew rate; Q = query output; diff = differential signals.

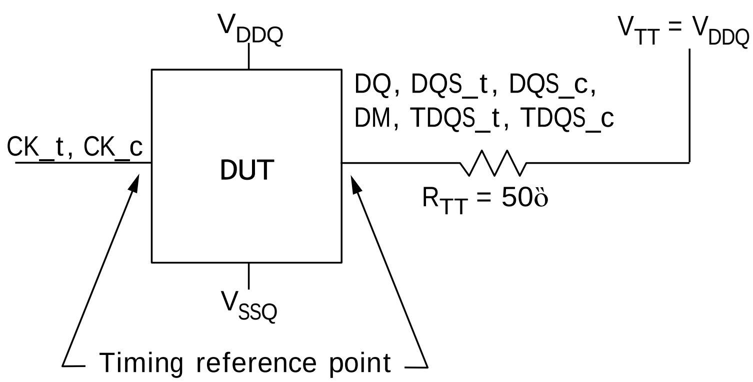
Reference Load for AC Timing and Output Slew Rate

The effective reference load of 50Ω to $V_{TT} = V_{DDQ}$ and driver impedance of $R_{ZQ}/7$ for each output was used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

R_{ON} nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing paraeter values of the device. The maximum DC high level of output signal = 1.0 × V_{DDQ}, the minimum DC low level of output signal = { 34 /(34 + 50) } × V_{DDQ} = 0.4 × V_{DDQ}

The nominal reference level of an output signal can be approximated by the following: The center of maximum DC high and minimum DC low = { (1 + 0.4) / 2 } × V_{DDQ} = 0.7 × V_{DDQ}. The actual reference level of output signal might vary with driver R_{ON} and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye.

Figure 5: Reference Load For AC Timing and Output Slew Rate



Electrical Specifications - I_{CDD} Parameters

Table 13: DDR4 I_{CDD} Specifications and Conditions - (0°≤ T_C ≤ 85°C)

Combined Symbol	Individual Die Status	Bus Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Units
I_{CDD0}	I_{CDD0} = I_{DD0} + I_{DD2P}	x4	89	90	91	92	93	mA
		x8	94	95	96	97	98	
I_{CPP0}	I_{CPP0} = I_{PP0} + I_{PP3N}	x4, x8	5	5	5	5	5	mA
I_{CDD1}	I_{CDD1} = I_{DD1} + I_{DD2P}	x4	100	101	102	103	104	mA
		x8	105	106	107	108	109	
I_{CDD2N}	I_{CDD2N} = I_{DD2N} + I_{DD2P}	x4, x8	79	80	81	82	83	mA
I_{CDD2NT}	I_{CDD2NT} = I_{DD2NT} + I_{DD2P}	x4, x8	85	86	87	88	89	mA
I_{CDD2P}	I_{CDD2P} = I_{DD2P} + I_{DD2P}	x4, x8	76	76	76	76	76	mA

Table 13: DDR4 I_{CDD} Specifications and Conditions - (0°≤ T_C ≤ 85°C)

Combined Symbol	Individual Die Status	Bus Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Units
I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P}$	x4, x8	80	80	80	80	80	mA
I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P}$	x4	94	95	96	97	98	mA
		x8	95	96	97	98	99	
I_{CPP3N}	$I_{CPP3N} = I_{PP3N} + I_{PP3N}$	x4, x8	4	4	4	4	4	mA
I_{CDD3P}	$I_{CDD3P} = I_{DD3P} + I_{DD2P}$	x4	82	83	84	85	86	mA
		x8	84	85	86	87	88	
I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{DD2P}$	x4	139	144	150	157	165	mA
		x8	147	155	163	170	178	
I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P}$	x4	118	122	126	130	134	mA
		x8	130	135	140	145	150	
I_{CDD5R}	$I_{CDD5R} = I_{DD5R} + I_{DD2P}$	x4, x8	106	106	106	106	106	mA
I_{CPP5R}	$I_{CPP5R} = I_{PP5R} + I_{PP3N}$	x4, x8	6	6	6	6	6	mA
I_{CDD6N}	$I_{CDD6N} = I_{DD6N} + I_{DD6N}$	x4, x8	106	106	106	106	106	mA
I_{CDD6E}[2]	$I_{CDD6E} = I_{DD6E} + I_{DD6E}$	x4, x8	180	180	180	180	180	mA
I_{CDD6R}[2]	$I_{CDD6R} = I_{DD6R} + I_{DD6R}$	x4, x8	40	40	40	40	40	mA
I_{CDD6A} (25°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	22	22	22	22	22	mA
I_{CDD6A} (45°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	40	40	40	40	40	mA
I_{CDD6A} (75°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	102	102	102	102	102	mA
I_{CDD6A} (95°C)[2]	$I_{CDD6A} = I_{DD6A} + I_{DD6A}$	x4, x8	180	180	180	180	180	mA
I_{CPP6X}	$I_{CPP6x} = I_{PP6x} + I_{PP6x}$	x4, x8	12	12	12	12	12	mA
I_{CDD7}	$I_{CDD7} = I_{DD7} + I_{DD2P}$	x4	248	263	278	293	308	mA
		x8	197	199	201	203	205	
I_{CPP7}	$I_{CPP7} = I_{PP7} + I_{PP3N}$	x4	13	13	13	13	13	mA
		x8	10	10	10	10	10	
I_{CDD8}	$I_{CDD8} = I_{DD8} + I_{DD8}$	x4, x8	72	72	72	72	72	mA

Notes: 1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.

2. I_{CDD6R} , I_{CDD6A}, and I_{CDD6E} values are verified by design and characterization, and may not be subject to production test.

3. I_{CDD} values must be derated (increased) when operated outside of the range 0°C ≤ T_C ≤ 85°C. They must also be derated when using features such as CAL, CA Parity, Read/Write DBI, AL, Gear-down, Write CRC, 2X/4X REF, and DLL disabled. Refer to the 16Gb monolithic data sheet for all derating values. Derating values apply to each individual I_{DDx} that make up the combined I_{CDD}

DRAM Package Electrical Specifications

Table 14: DRAM Package Electrical Specifications for x4, x8, and x16 DDP Devices

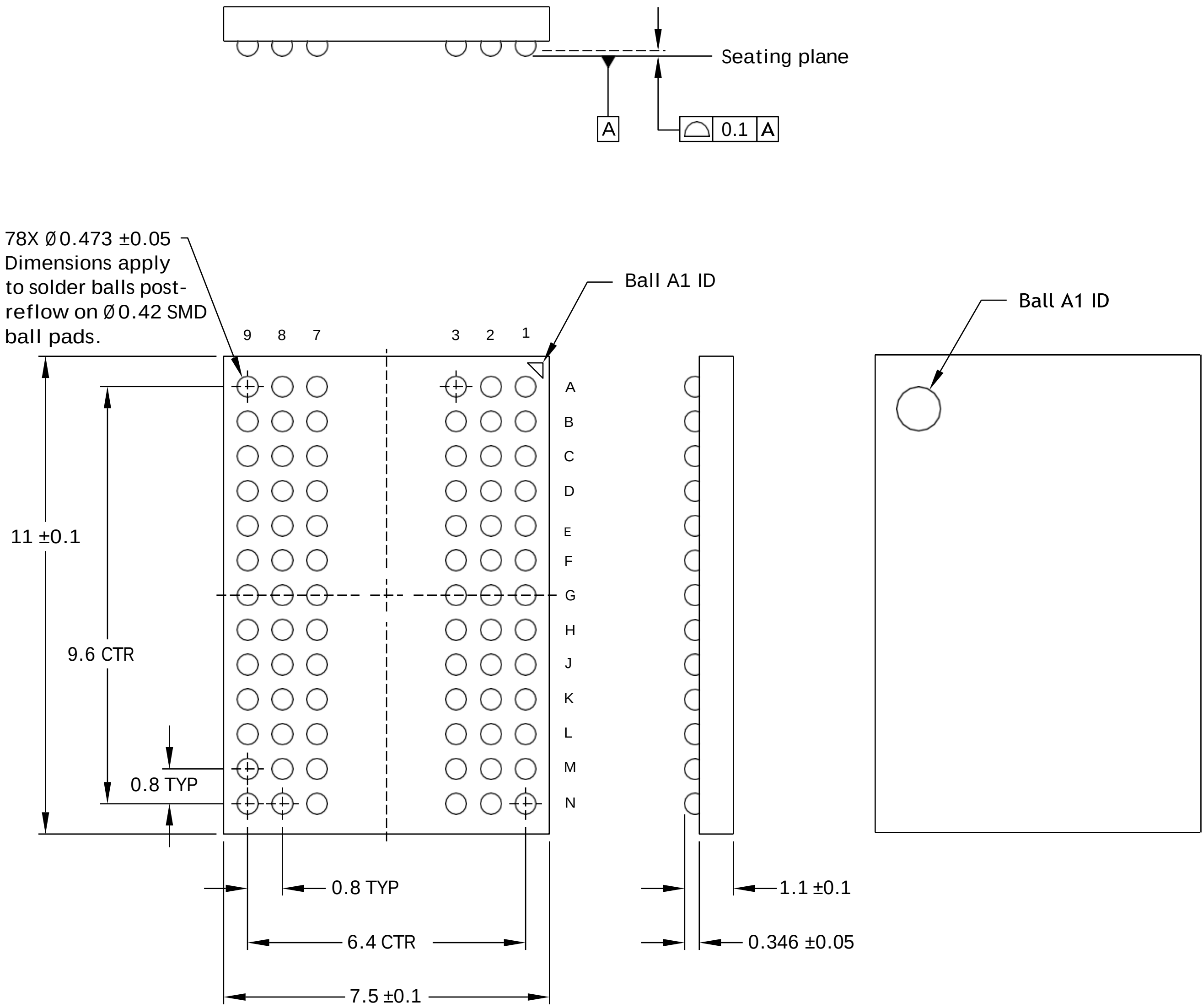
Parameter		Symbol	DDR4-1600, 1866, 2133, 2400, 2666, 2933, 3200 Min	Max	Unit	Notes
Input/output	Zpkg	Z_{IO}	35	60	ohm	3
	Package delay	Td_{IO}	60	120	ps	3
	Lpkg	L_{IO}	-	5.5	nH	
	Cpkg	C_{IO}	-	4	pF	
DQSL_t/DQSL_c/DQSU_t/DQSU_c	Zpkg	$Z_{IO\ DQS}$	35	60	ohm	
	Package delay	$Td_{IO\ DQS}$	60	120	ps	
	Lpkg	$L_{IO\ DQS}$	-	5.5	nH	
	Cpkg	$C_{IO\ DQS}$	-	4	pF	
DQSL_t/DQSL_c, DQSU_t/DQSU_c,	Delta Zpkg	$DZ_{IO\ DQS}$	-	5	ohm	4
	Delta delay	$DTd_{IO\ DQS}$	-	5	ps	4
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	30	70	ohm	5
	Package delay	$Td_{I\ CTRL}$	60	120	ps	5
	Lpkg	$L_{I\ CTRL}$	-	7.5	nH	
	Cpkg	$C_{I\ CTRL}$	-	4	pF	
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	30	60	ohm	6
	Package delay	$Td_{I\ ADD\ CMD}$	60	120	ps	6
	Lpkg	$L_{I\ ADD\ CMD}$	-	7.5	nH	
	Cpkg	$C_{I\ ADD\ CMD}$	-	4	pF	
CK_t, CK_c	Zpkg	Z_{CK}	30	60	ohm	
	Package delay	Td_{CK}	60	120	ps	
	Delta Zpkg	DZ_{DCK}	-	5	ohm	7
	Delta delay	DTd_{DCK}	-	5	ps	7
Input CLK	Lpkg	$L_{I\ CLK}$	-	7.5	nH	
	Cpkg	$C_{I\ CLK}$	-	4	pF	
ZQ Zpkg		$Z_{O\ ZQ}$	-	50	ohm	
ZQ delay		$Td_{O\ ZQ}$	30	135	ps	
ALERT Zpkg		$Z_{O\ ALERT}$	30	60	ohm	
ALERT delay		$Td_{O\ ALERT}$	60	110	ps	

Notes: 1. The values in this table are guaranteed by design/simulation only, and are not subject to production testing.

2. Package implementations should satisfy targets if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown. The package design targets are provided for reference, system signal simulations should not use these values but use the Alliance package model.
3. Z_{IO} and Td_{IO} apply to DQ, DM, DQS_c, DQS_t, TDQS_t, and TDQS_c.
4. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
5. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, and CKE.
6. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], RAS_n CAS_n, and WE_n.
7. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
8. Notes 1-2 apply to the entire table.

Package Dimensions

Figure 6: 78-Ball FBGA



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SACQ (92.5% Sn, 3% Ag, 4% Bi, 0.5% Cu).

PART NUMBERING SYSTEM

AS4C	4G8D4	-62	B	C	N	XX
DRAM	4G8=4G x 8 D4=DDR4	62=1600 MHz	B=FBGA	C=Commercial temp 0°C~ 95°C	Indicates Pb and Halogen Free	Packing Type None:Tray TR:Reel

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