

3.5. Latch-Up Test

CMOS products can be prone to over-voltage exceeding the maximum device rating if the parasitic p-n-p-n SCRs (Silicon-controlled rectifier) are improperly biased. When the SCR turns on, it draws excessive current and causes products being damaged by thermal runaway. The Table 6 shows the latch-up test method and the test result of no failure.

Test Item	Test Method			Result (F/S.S)
	Reference Standard	Test Condition & Criteria	Sample	
Latch-Up	JESD78	$V_{tr(+)} \geq 1.5 * V_{cc}$ $V_{tr(-)} \leq -0.5 * V_{cc}$ $I_{tr(+)} \geq 100mA$ $I_{tr(-)} \leq -100mA$	6ea	0/6

Table 6. Latch-Up test Condition and Result

4. CONCLUSION

Reliability test is to ensure the ability of a product in order to perform a required function under specific conditions for a certain period of time. Through those tests, the devices of potential failure can be screened out before shipping to the customer. At the same time, the test results are fed back to process, design and other related departments for improving product quality and reliability.

According to the life time test data, *the short-term 12Hrs failure rate (= the normal operation 0-1 year) of AS4C4M16SA-5TCN / 7B2CN is equal to 0 DPM at Ta=55°C and Vcc=3.3V with 60% confidence level AND the long-term 1000Hrs failure rate (= the normal operation 1-10 year) of AS4C4M16SA-5TCN / 7B2CN is equal to 22 FIT at Ta=55°C and Vcc=3.3V with 60% confidence level.* The results of environmental test, ESD test and latch-up test also ensure that the AS4C4M16SA-5TCN / 7B2CN is manufactured under a precise control of quality work by Alliance and its subcontractors. ***Thus, this experiment based on the Alliance reliability test standard for above test items can all pass.***

With the extensive research and development activities and the cooperation of all departments, Alliance continuously sets and maintains higher standard of quality and reliability to satisfy the future demand of its customers.