

# Reliability Qualification Report

for

**Serial NOR Flash with Pb/Halogen  
Free (Industrial)**

**AS25F1128MQ-70SIN : 8SOP (208mils)**

**AS25F1128MQ-70WIN : 8 WSON (6x5mm)**

## Contents

### **1. Information**

### **2. Product Reliability Test Description**

### **3. Product Reliability Test Result**

3-1. Reliability Test Result

3-2. ESD Test Result

3-3. Latch up Test Result

3-4. Pre-condition Test Result

3-5. Estimation of hard error rate from HTOL

### **4. Attachment**

4-1. Product reliability qualification test summary

## 1. Information

### 1.1 Device Code

- AS25F1128MQ-70SIN

### 1.2 Design Information

- Design Rule : .65nm technology.
- Cell Size (6F<sup>2</sup>) : 0.15um x 0.3um = 0.045um<sup>2</sup>
- Chip Size ( with S/L: 60um) : 3,052 mm x 3,320 mm = 12.07mm<sup>2</sup>

### 1.3 Wafer Fabrication

- Foundry : SMIC
- Technology : 2 Poly / 3 Metal 65nm.
- Gate Oxide : 44 Å / 156 Å dual gate oxide
- Gate : n+ / p+ poly + Co-Salicide
- Metal : W / AlCu
- Top layer : Passivation UV SiN 6000 Å

### 1.4 Assembly

#### **Package : 8pin SOP 208-mils**

- Assembly house : GREATEK
- Test Location : ChipMOS.
- Lead frame : SHINKO A-194
- Molding compound : Sumitomo G700
- Wire Material : TANAKA 4N

#### **Package : 8L WSON (6x5x0.85mm)**

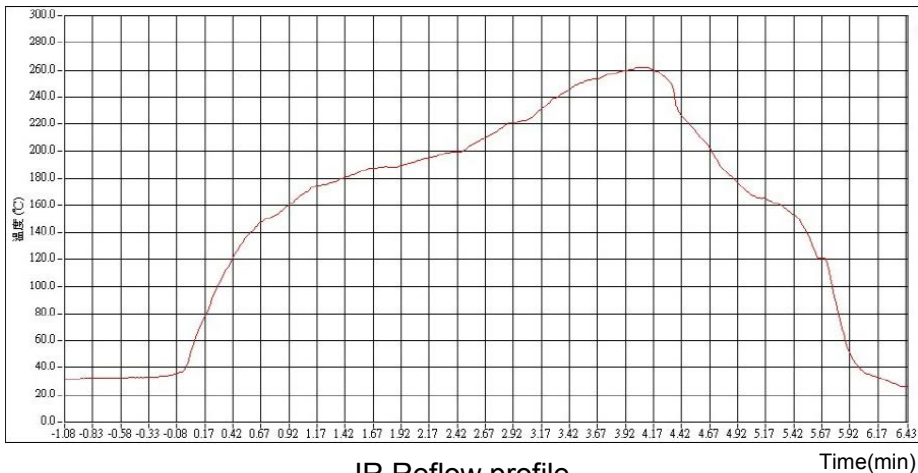
- Assembly house : GREATEK
- Test Location : ChipMOS.
- Lead frame : A194
- Molding compound : Sumitomo G700H
- Wire Material : TANAKA 4N
- Lead Finish : Pure Tin

## 2. Product Reliability Test Description

Test item	Test Condition	Reference	SS(ea)	Acceptance Criteria	
EFR	125°C, VCC=2.2V VIH=1.95V, Dynamic	JESD22A108 JESD74	5400ea	1000ppm	
HTOL	125°C, VCC=2.2V VIH=1.95V, Dynamic	JESD22A108	300ea	0fail	
Endurance	85°C, VCC=2.2V VIH=1.95V	JESD22A117	231ea	0fail	
HTS	150°C	JESD22A103	180ea	0fail	
TC	-65°C/150°C	JESD22A104	180ea	0fail	
PCT	121°C/100%RH 30psia	JESD22A102	180ea	0fail	
THB	85°C/85%RH, VCC * 1.2	JESD22A101	135ea	0fail	
HAST	130°C/85%RH 33.3psia, VCC * 1.2	JESD22A110	180ea	0fail	
ESD	HBM C=100pF, R=1.5K 3 times stressing Forward each pin against Vss or Vcc	MIL-STD-883F	9ea	0fail	
	CDM	Field	JESD22C101	9ea	0fail
		Direct	ESDASTM 5.3.1	9ea	0fail
	MM C=200pF 3 times stressing Forward each pin against Vss or Vcc	JESD22A115	9ea	0fail	
Latch up	I-test	JESD78	18ea	0fail	
	V-test				Positive
Precon	Refer to below	JESD22A113	675ea	0fail	

❖ With Precondition as follows :

T/C 5 cycle → T/H 192hrs → IR reflow ( 3times )  
 ( -65°C/150°C ) ( 30°C/60%RH ) ( T peak = 260°C )



IR Reflow profile

## 3. Test Results Summary

### 3-1. Test Result Summary

Item	Result			
	Test Results	QFAEP2174	QFAEP2173	QFAEP2172
EFR	0/5400	0/1800	0/1800	0/1800

Item	Result			
	Lot Number	168hrs	504hrs	1008hrs
HTOL	QFAEP2174	0/100	0/100	0/100
	QFAEP2173	0/100	0/100	0/100
	QFAEP2172	0/100	0/100	0/100

Item	Result				
	Lot Number	10kcycles	20kcycles	50kcycles	100kcycles
Endurance (85°C)	QFAEP2174	0/77	0/77	0/77	0/77
	QFAEP2173	0/77	0/77	0/77	0/77
	QFAEP2172	0/77	0/77	0/77	0/77

Item	Result			
	After Pre-condition	168hrs	504hrs	1008hrs
HTS	N.A	0/180	0/180	0/180

Item	Result			
	After Pre-condition	200 Cycles	500 Cycles	700 Cycles
T/C	N/A	0/180	0/180	0/180

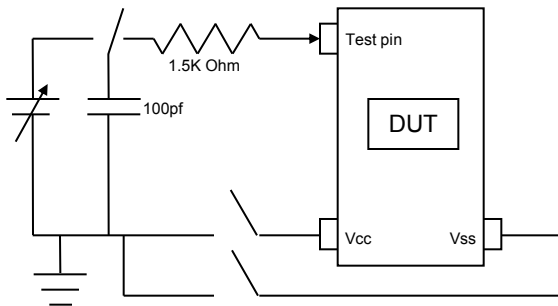
Item	Result		
	After Pre-condition	96hrs	168hrs
PCT	N/A	0/180	0/180

Item	Result			
	After Pre-condition	168hrs	504hrs	1008hrs
THB	N/A	0/135	0/135	0/135

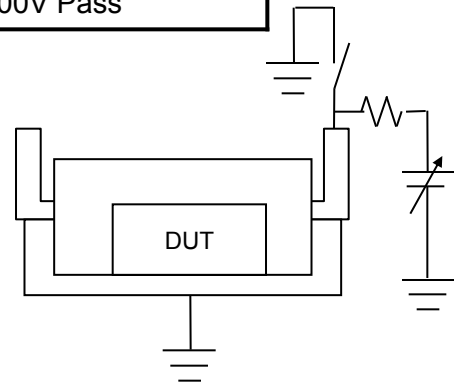
Item	Result		
	After Pre-condition	48hrs	96hrs
HAST	N/A	0/180	0/180

### 3-2. ESD Test Result Summary

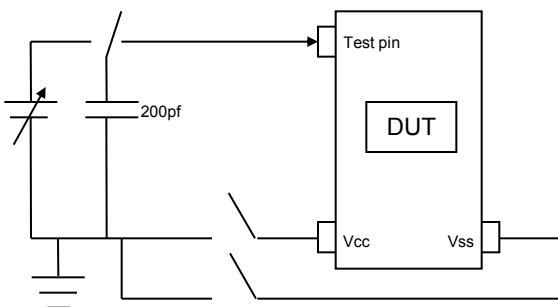
Item	Results
HBM ( $\pm 2000V$ )	Pass (0/9, 3lots) 2000V Pass
MM ( $\pm 200V$ )	Pass (0/9, 3lots) 200V Pass
CDM ( $\pm 1000V$ )	Pass (0/9, 3lots) 1000V Pass



**Fig 3-2-1 Test Circuit of HBM**



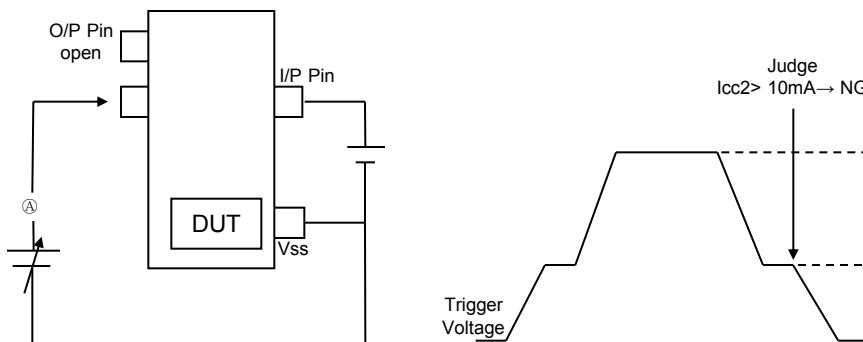
**Fig 3-2-2 Test Circuit of CDM**



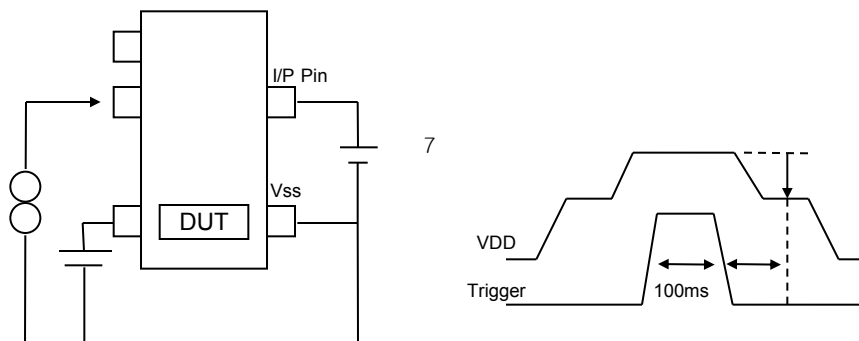
**Fig 3-2-3 Test Circuit of MM**

## 3-3. Latch-up immunity

Item	Input Pin Level	Measurement Pin	Test Condition	Latch-up Voltage & Current
				Result
Vcc Pin	Vcc	Vcc (see Fig 3-3-1)	Vcc, over $\geq 3.0V$ Temp=85°C	Pass(0/9, 3 lots) $\geq 3.0V$
	GND			
Input Pin	Vcc	Input (see Fig 3-3-2)	Icc, trig $\geq \pm 150mA$ Temp = 85°C	Pass(0/9, 3 lots) $> \pm 150mA$
	GND			
Output Pin	Vcc	Output ( see Fig 3-3-2)		Pass(0/9, 3 lots) $> \pm 150mA$
	GND			



**Fig 3-3-1 Set up of Power Supply Over Voltage Latch-up test**



**Fig 3-3-2 Set up of Current Injection Latch-up test**

## 3-4. Pre-condition Result

Item	Result
Pre-Con	Pass Level III (0/675)



## Estimation of hard error rate from HTOL

### 1. Acceleration factor

To Estimate of hard error rate from EFR and HTOL, we assumed the acceleration factors as follows:

Thermal Acceleration Factor :  $AF_{th} = \exp(Ea/K_B) \cdot [(1/T_{c\_use}) - (1/T_{c\_stress})]$

$$Ea = 0.77\text{eV}, T_{c\_use} = 85^\circ\text{C}, T_{c\_stress} = 125^\circ\text{C}, K_B = 8.62 \cdot 10^{-5} \text{ eV/K}$$

Electrical Acceleration Factor :  $AF_{el} = \exp[\beta(V_{stress} - V_{use})]$

$$\beta = 3.82, VCC_{use} = 1.95\text{V}, VCC_{stress} = 2.2 \text{ V(EFR)}, 2.2 \text{ V(HTOL)}$$

Where

$Ea$  : Activation Energy(eV)

$K_B$  : Boltzman constant( $8.62 \cdot 10^{-5}$  eV/K)

$T$  : Absolute temperature(K)

$\beta$  : Voltage acceleration factor(1/V)

### 2. Hard Error Rate Estimated

- 1.8 V power supply products
- Actual usage condition ;  $T_{c\_use} = 85^\circ\text{C}$ ,  $VCC_{use} = 1.95\text{V}$
- Test condition :

$$T_{c\_stress} = 125^\circ\text{C}, VCC_{stress} = 2.0\text{V(EFR)}, 2.0\text{V(HTOL)},$$

Assuming that failure time depend on exponential and weibull distribution.

Thermal acceleration :  $AF_{th} = 12.27$  ( $T_{c\_use} = 85^\circ\text{C} \rightarrow T_{c\_stress} = 125^\circ\text{C}$ )

Electrical acceleration of EFR :  $AF_{el(EFR)} = 2.60$  ( $VCC_{use} = 1.95\text{V} \rightarrow VCC_{stress} = 2.2\text{V}$ )

Electrical acceleration of HTOL :  $AF_{el(HTOL)} = 2.60$  ( $VCC_{use} = 1.95\text{V} \rightarrow VCC_{stress} = 2.2\text{V}$ )

Total acceleration of EFR =  $AF_{th} \times AF_{el(EFR)} = 31.88$

Total acceleration of HTOL =  $AF_{th} \times AF_{el(HTOL)} = 31.88$

Hard Error Rate = (failure count at confidential level = 60%) $\cdot 10^9 / (2 \cdot (\text{Device hours}) \cdot AF)$

, where device hours from HTOL stress is sample size multiplied by stress time, and voltage and temperature acceleration factors.

Duration	Sample Size	No. of Failure	FIT (C.L.=60%)	MTTF (years)
168H	300	0	570	200
504H	300	0	190	600
1008H	300	0	95	1200

## Product reliability qualification test result

Test items	Conditions	Samples	No of fail
EFR	Ta = 125°C, VCC = 2.2V 48hrs	1800 * 3	0
HTOL Test	Ta = 125°C, VCC = 2.2V 1008hrs	100 * 3	0
Endurance	85°C, VCC=2.2V, 100k cycle	77 * 3	0
HTS Test	Ta= 150°C 1008hrs	45 * 4	0
TC Test	-65°C / 150°C* 700cycle	45 * 4	0
HAST Test	130°C / 85% RH VCC * 1.2 t = 96hrs	45 * 4	0
THB Test	85°C / 85% RH VCC * 1.2 1008hrs	45 * 3	0
PCT Test	Ta=121°C, 30psi 100% RH, 168hrs	45 * 4	0
ESD Test	HBM V=±2000V	3 * 3	0
	MM V=±200V	3 * 3	0
	CDM V=±1000V	3 * 3	0
Latch-up Test	Current Injection I = ± 150mA	3 * 3	0
	PSOV = ± 3.0V	3 * 3	0
Pre-condition	Temp. cycle(-65°C/150°C,5cycle)+ Soak (30°C/60%RH,192hrs)+ IR Reflow(250°C, 3 times)	675	0