4M SRAM
44L TSOP II(400mil)
Reliability Test Report

Device No. :	AS6C4016B-45ZIN
Description :	4M (256KX16) Bits Low Power SRAM
Prepared by :	QRA Dept.
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(1.) Introduction

This report provides an overview of the reliability test conditions and results of Low Power 256Kx16 CMOS SRAM. In ALLIANCE MEMORY, the basic policy is to maintain electrical characteristics within the limits established in the specifications of each device.

(2.) Product information

The AS6C4016B-45ZIN is a 256Kx16 bits low power CMOS static random access memory. It is fabricated using high performance, high reliability CMOS technology. The AS6C4016B-45ZIN operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

The following is the basic process and package information of this device.

L/F material	A42 / C7025 / EFTEC64T	
Wire Bond material	Au φ23um Cu φ20/23um	
Package material	Lead Free (Green)	
Lead Finish	Pure Sn (100% Matte Tin)	
Die attach adhesive	Hitachi EN-4900 / Sumitomo CRM-1076	
Molding compound	Hitachi CEL-9200HF	Sumitomo MEM-G631

(3.) Reliability Test Result

(3.1) Life Tests

*HTOL：

HTOL is a "high temperature operating life" test .All memory cells were written with march pattern at Vcc_max=4.8V and ambient temperature = 125℃ during HTOL test. The data for this test is presented in the following table:

Test Method			Result	
Reference Standard	Test Condition	LTPD %	Samples	Fails
JEDEC-STD-22-A108	Vcc_max=4.8V Temp.=125°C 1000 hrs	5	77 (I665714A0552O)	0
			80 (I895534B0231O)	0
			80 (I666429C1131O)	0

FAILURE RATE CALCULATION

Accelerated test would expose any possible design and process flaws, it is also used to predict failure rates through the Arrhenius Equation under normal operation.

Acceleration factor(AF)

AF(Temperature) = exp[(Ea/K)(1/T1 – 1/T2)]
Ea : activation energy
K : Boltzman constant(8.62*E-5 eV/K)
T1 : max. operating temperature(absolute temperature K)
T2 : stress temperature(absolute temperature K)

AF(voltage) =exp(βΔV)
β: constant that is function of dielectric type and thickness
ΔV : stress voltage - max. operating voltage

So; the acceleration factor (AF)=AF(temperature)*AF(voltage)

Sample calculation with Ea=0.69 eV
AFT(125℃,70℃)=25.15
AFV(4.8V,3.6V)=37.94

AF(total)=AF(temperature)*AF(voltage)=954.30

$$\text{Failure Rate(F.R.) } = [X^2(1\text{-CL},2N+2)]/2EDH \text{ (FIT)}]$$

X^2 : CHI SQUARE Function
CL: Confidence Level
N : No of Failure
EDH : Equivalent Device Hour

Test item	Device Hours at Temp.=125 ºC Vcc =4.8 V	Device Hours At Temp.=70 ºC Vcc =3.6 V	No of Failed / sample size	Failure rate at 70 ºC
HTOL	237000	2.26E+08	0/237	4.05 FIT

Based on CL=60%

(3.2) Environmental Tests

The purpose of environmental test is to measure the device that resists to exposure at high and low temperature, and high humidity conditions.

a) Temperature Cycling Test (TCT)

The purpose of temperature cycle testing is to study the effect of thermal expansion mismatch among the different component with in a specific die and package system. Such as wire bond, die bond and package irregularities, die crack …etc. The data for this test is presented in the following table:

Test Method			Result	
Reference Standard	Test Condition	LTPD %	Samples	Fails
JEDEC-STD-22-A104	-65ºC to 150ºC 24 min/cycle 500 cycle	5	77 (IL01006A0430S)	0
			77 (I188580L0631S)	0
			77 (IL23059F0330S)	0
			77 (I213589O05W4S)	0
			77 (I665714B1531S)	0

b) Thermal Shock Test (TST)

Thermal shock testing is similar to TCT (temperature cycling test), except that in thermal shock tests an additional stress is provided: a sudden change in temperature due to a rapid transfer time. Thus this test can detect failure mechanisms caused by temperature transient and temperature gradient. The data for this test is presented in the following table:

Test Method			Result	
Reference Standard	Test Condition	LTPD %	Samples	Fails
JEDEC-STD-22-A106	-65ºC to 150ºC 11 min/cycle 500 cycle	5	45 (IA684555D6F4C)	0
			45 (CYC18370A430C)	0
			77 (IA899370BX30C)	0
			45 (IA899391A23PH)	0

c) Pressure Cooker Test (PCT)

PCT test is performed to evaluate the moisture resistance of non-hermetic packaged units. Devices are subject to pressure, humidity, and elevated temperature to accelerate the penetration of moisture through the molding compound or along the interface of the device pins and molding compound. The data for this test is presented in the following table:

Test Method			Result	
Reference Standard	Test Condition	LTPD %	Samples	Fails
JEDEC-STD-22-A102	2 atms 121℃/100%RH 168 hrs	5	77 (C152067J0231S)	0
			77 (IL01006A0430S)	0
			77 (I188580L0631S)	0
			77 (IL23059F0330S)	0
			77 (I213589O05W4S)	0

e) Highly Accelerated Stress Test (HAST)

HAST is performed to evaluate the non-hermetic packaging of solid state equipment in humid environments. HAST accelerates the penetration of moisture through the external protective material or at the seals around the chip leads.

The data for this test is presented in the following table:

Test Method			Result	
Reference Standard	Test Condition	LTPD %	Samples	Fails
JEDEC-STD-22-A110	2 atms 130℃/85%RH no bias 168 hrs	5	77 (IL01006A0430S)	0
			77 (I188580L0631S)	0
			77 (IL23059F0330S)	0
			77 (I213589O05W4S)	0
			77 (I665714B1531S)	0

f) High Temperature Storage Test (HTST)

HTSL is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. The data for this test is presented in the following table:

Test Method			Result	
Reference Standard	Test Condition	LTPD %	Samples	Fails
JEDEC-STD-22-A103	Temperature: 150℃ Read out: 1000 hrs	5	77 (IK47048C0230S)	0
		5	77 (IM35321D023AS)	0
		5	77 (IM11517D0330S)	0
		5	77 (I213589O05W4S)	0
		5	77 (I665714B1531S)	0

(3.3) ESD Test

Test Item	Test Method				Result
	Reference Standard	Test Condition	Calss	Sample	
H.B.M.	JEDEC-STD-22-A114	R=1.5 Kohm C=100 pF	3A	18	0/18 >±4.0KV
M.M.	JEDEC-STD-22-A115	R=0 ohm C=200 pF	C	18	0/18 >±400V
C.D.M	JESD22-C101	Without socket	III	12	0/12 >±800V

(3.4) Latch-up Test

Test Item	Test Method				Result
	Reference Standard	Test Condition	Class	Sample	
Latch-Up	JEDEC-STD-78 (With socket)	Current trigger	I	11	0/11 >±400mA
		Voltage trigger		3	0/3 >5.55V

(3.5) Solderability Test

Solderability test is to evaluate device package be joined to another surface using solder.

The data for this test is presented in the following table:

Test Method		Result	
Reference Standard	Test Condition	Samples	Fails
JEDEC STD-22-B102 JEDEC STD-002 MIL-STD-883E-2003	1. Sn / 3.0Ag / 0.5Cu 2. Steam aging: 8hrs (93°C/100% R.H./1atm) 3. 245±5°C, 5 sec. >95% solder covering	5 (I153623M0264O)	0
		5 (IA661383C664C)	0
		5 (I213589O05W4S)	0
		5 (IV42187F0830S)	0
		5 (IU14382B0330S)	0

Appendix

Reversion History

Rev.	Effective Date	Init.	Description of Changing
A	Mar.15.2023	QRA	Initial Issue.