# 4M SRAM
# 48L BGA
# Reliability Test Report

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|---|---|
| Device No. : | AS6C4016B-45BIN |
| Description : | 4M (256KX16) Bits Low Power SRAM |
| Approved Date : | 2023.03.15 |
| Document No : | 310-9N8-AG4 Rev : A |

## (1.) Introduction

This report provides an overview of the reliability test conditions and results of Low Power 256Kx16 CMOS SRAM. In ALLIANCE MEMORY, the basic policy is to maintain electrical characteristics within the limits established in the specifications of each device.

## (2.) Product information

The AS6C4016B-45BIN is a 256Kx16 bits low power CMOS static random access memory. It is fabricated using high performance, high reliability CMOS technology. The AS6C4016B-45BIN operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

The following is the basic process and package information of this device.

| | | | |
|---|---|---|---|
| L/F material | CCL-HL832NX | | |
| Wire Bond material | Au φ23/20um | | |
| Package material | Lead Free (Green) | | |
| Lead Finish | 96.5Sn / 3Ag / 0.5Cu | | |
| Die attach adhesive | Henkel/Ablestik 2025D<br>Nitto EM-700/ EM-310/EM-710(760) | | |
| Molding compound | Shin Etsu KMC-3520 | Kyocera KE-G1250 | Sumitomo E770 |

## (3.) Reliability Test Result

### (3.1) Life Tests

*HTOL;

HTOL is a "high temperature operating life" test .All memory cells were written with march pattern at Vcc_max=4.8V and ambient temperature = 125℃ during HTOL test. The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A108 | Vcc_max=4.8V<br>Temp.=125°C<br>1000 hrs | 5 | 77<br>(I665714A0552O) | 0 |
| | | | 80<br>(I895534B0231O) | 0 |
| | | | 80<br>(I666429C1131O) | 0 |

## FAILURE RATE CALCULATION

Accelerated test would expose any possible design and process flaws, it is also used to predict failure rates through the Arrhenius Equation under normal operation.

Acceleration factor(AF)

AF(Temperature) = exp[(Ea/K)(1/T1 – 1/T2)]
Ea : activation energy
K : Boltzman constant(8.62*E-5 eV/K)
T1 : max. operating temperature(absolute temperature K)
T2 : stress temperature(absolute temperature K)

AF(voltage) =exp(βΔV)
β: constant that is function of dielectric type and thickness
ΔV : stress voltage - max. operating voltage

So; the acceleration factor (AF)=AF(temperature)*AF(voltage)

Sample calculation with Ea=0.69 eV
AFT(125℃,70℃)=25.15
AFV(4.8V,3.6V)=37.94

AF(total)=AF(temperature)*AF(voltage)=954.30

$$\text{Failure Rate( F.R.) } = [X^2(1\text{-CL},2N+2)]/2EDH \text{ (FIT)}]$$

$X^2$ : CHI SQUARE Function
CL: Confidence Level
N : No of Failure
EDH : Equivalent Device Hour

| Test item | Device Hours at Temp.=125 ºC Vcc =4.8 V | Device Hours At Temp.=70 ºC Vcc =3.6 V | No of Failed / sample size | Failure rate at 70 ºC |
|---|---|---|---|---|
| HTOL | 237000 | 2.26E+08 | 0/237 | 4.05 FIT |

Based on CL=60%

## (3.2) Environmental Tests

The purpose of environmental test is to measure the device that resists to exposure at high and low temperature, and high humidity conditions.

### a) Temperature Cycling Test (TCT)

The purpose of temperature cycle testing is to study the effect of thermal expansion mismatch among the different component with in a specific die and package system. Such as wire bond, die bond and package irregularities, die crack …etc. The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A104 | 2 atm<br>121℃/100%RH<br>168 hrs | 5 | 77<br>(IT32038O0334C) | 0 |
| | | | 77<br>(I757704E1034C) | 0 |
| | | | 77<br>(I666288B0934C) | 0 |
| | | | 45<br>(I794040E0234S) | 0 |
| | | | 45<br>(I794040E0334S) | 0 |

### b) Thermal Shock Test (TST)

Thermal shock testing is similar to TCT (temperature cycling test), except that in thermal shock tests an additional stress is provided: a sudden change in temperature due to a rapid transfer time. Thus this test can detect failure mechanisms caused by temperature transient and temperature gradient. The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A106 | -65°C to 150°C<br>11 min/cycle<br>500 cycle | 5 | 45<br>(CA680884F150C) | 0 |
| | | | 45<br>(CA680884F630C) | 0 |
| | | | 45<br>(CA680686F150C) | 0 |

**c) Pressure Cooker Test (PCT)**

PCT test is performed to evaluate the moisture resistance of non-hermetic packaged units. Devices are subject to pressure, humidity, and elevated temperature to accelerate the penetration of moisture through the molding compound or along the interface of the device pins and molding compound. The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A102 | 2 atm<br>121℃/100%RH<br>168 hrs | 5 | 77<br>(IK47044D0330C) | 0 |
| | | | 77<br>(IM11517D0630S) | 0 |
| | | | 77<br>(IK42166E0231O) | 0 |
| | | | 45<br>(I665279E0934O) | 0 |
| | | | 77<br>(IM49002F0430S) | 0 |

**d) High Temperature and high Humidity Test (THT)**

THT testing is a reliability test designed to accelerate metal corrosion particularly that of the metallization on the die surface of the device. The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A101 | 85℃/85%RH<br>1000 hrs | 5 | 45<br>(CA686842C231C) | 0 |

**e ) Highly Accelerated Stress Test (HAST)**

HAST is performed to evaluate the non-hermetic packaging of solid state equipment in humid environments. HAST accelerates the penetration of moisture through the external protective material or at the seals around the chip leads.

The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A110 | 2 atms<br>130℃/85%RH<br>No Bias<br>168 hrs | 5 | 77<br>(IT32038O0334C) | 0 |
| | | | 77<br>(I757704E1034C) | 0 |
| | | | 77<br>(I666288B0934C) | 0 |
| | | | 45<br>(I794040E0234S) | 0 |
| | | | 45<br>(I794040E0334S) | 0 |

**f) High Temperature Storage Test (HTST)**

HTSL is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied. The data for this test is presented in the following table:

| Test Method | | | Result | |
|---|---|---|---|---|
| Reference Standard | Test Condition | LTPD % | Samples | Fails |
| JEDEC-STD-22-A103 | Temperature: 150℃<br>Read out: 1000 hrs | 5 | 77<br>(IT32038O0334C) | 0 |
| | | | 77<br>(I757704E1034C) | 0 |
| | | | 77<br>(I666288B0934C) | 0 |
| | | | 45<br>(I794040E0234S) | 0 |
| | | | 45<br>(I794040E0334S) | 0 |

**(3.3) ESD Test**

| Test Item | Test Method | | | | Result |
|---|---|---|---|---|---|
| | Reference Standard | Test Condition | Calss | Sample | |
| H.B.M. | JEDEC-STD-22-A114 | R=1.5 Kohm<br>C=100 pF | 3A | 18 | 0/18<br>>±4.0KV |
| M.M. | JEDEC-STD-22-A115 | R=0 ohm<br>C=200 pF | C | 18 | 0/18<br>>±400V |
| C.D.M | JESD22-C101 | Without socket | III | 12 | 0/12<br>>±800V |

**(3.4) Latch-up Test**

| Test Item | Test Method | | | | Result |
|---|---|---|---|---|---|
| | Reference Standard | Test Condition | Class | Sample | |
| Latch-Up | JEDEC-STD-78<br>(With socket) | Current trigger | I | 11 | 0/11<br>>±400mA |
| | | Voltage trigger | | 3 | 0/3<br>>5.55V |

## Appendix

### Reversion History

| Rev. | Effective Date | Init. | Description of Changing |
|---|---|---|---|
| A | Mar.15.2023 | QRA | Initial Issue. |