

for

LPSDR SDRAM with Pb/Halogen Free (Industrial)

(16M×16, 45nm SDRAM AS4C16M16MSB-6BIN)



Contents:

- 1. Title
- 2. Product and Package Information
- 3. Result Summary
- 4. Accelerated Lifetime Simulation Tests (Including Failure Rate Estimation)
- 5. Accelerated Environment Stress Tests
- 6. Electrical Verification Tests (Electrostatic Discharge & Latch-up)



1. Title

This report describes the reliability and qualification data of Alliance product listed below. The reliability tests have been completed successfully based on Alliance standard.

2. Product and Package Information

Product Code : AS4C16M16MSB-6BIN

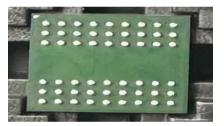
Product Description : 256Mb LPSDR Operating Temperature Range : -40°C to +85°C

Operating Voltage : VDD/VDDQ 1.7~1.95V

Package Type : FBGA 54B (8.0x8.0mm, 1.0T)

Flammability : UL-V0





3. Result Summary

Process Results : Pass All Items

Lifetime Simulation Tests : Pass ELFR & HTOL

Environment Stress Tests : Pass All Tests Environment Compliance : Meet All Items



4. Accelerated Lifetime Simulation Tests

Ī	Group	Test Item / Conditions	Test Method	Duration or Level	Result		
					Number of Lots	Failed Q'ty / Tested Q'ty	Notes
	-ifetime Simulatic	Early Life Failure Rate 125°C, VDD/VDDQ/VPP Dynamic stress	JESD22-A108	48 hours	1	0 / 2300 (Pass)	1, 2
		High Temperature Operating Life 125°C, VDD/VDDQ/VPP Dynamic stress	JESD22-A108	1008 hours	1	0 / 231 (Pass)	1, 2

Note:

- 1) Electrical test is performed before and after each item.
- 2) "Dynamic stress" means continuous memory operation like read or write function.

* Failure Rate Estimation

Estimation Condition:

User Operating Temperature: 55°C

User Operating Voltage : Typical VPP

Operating Voltage : VDD/VDDQ & VPP

Confidence Level

 $AF_{OVERALL} = AF_{T} * AF_{V} = 22.5 * 7.92 = 178$

Early Life (Ea = 0.5 eV, $\beta = 6.9$) : 46.6 FITs Inherent Life (Ea = 0.5 eV, $\beta = 6.9$): 17.0 FITs

5. Accelerated Environment Stress Tests

	Test Item Test / Conditions Method	Tool	Duration or Level	Result		
Group				Number of Lots	Failed Q'ty / Tested Q'ty	Notes
sts	Preconditioning Temperature Cycling: -55°C to 125°C Bake: 125°C Soak: 30°C, 60% RH Reflow: 260°C	JESD22-A113	Level 3 5 cycles 24 hours 192 hours 3 cycles	1	0 / 225 (Pass)	1
Stress Te	Temperature & Humidity 85°C, 85% RH	JESD22-A101	504 hours	1	0 / 75 (Pass)	1, 2
ironment	Temperature Cycling -50°C to 125°C	JESD22-A104	1000 cycles	1	0 / 75 (Pass)	1, 2
Accelerated Environment Stress Tests	Pressure Cooker Test 121°C, 100%RH, 2ATM	JESD22-A102	168 hours	1	0 / 75 (Pass)	1, 2
Accele	Low Temperature Storage Life -50°C	JESD22-A119	1008 hours	1	0 / 75 (Pass)	1
	High Temperature Storage Life 150°C	JESD22-A103	1008 hours	1	0 / 75 (Pass)	1

Note

- 1) Electrical test is performed before and after each item.
- 2) Preconditioning is performed before the test.



6. Electrical Verification Tests (Electrostatic Discharge & Latch-up)

	Test Item / Conditions	Test Method	Duration or Level	Result		
Group				Number of Lots	Failed Q'ty / Tested Q'ty	Notes
ests	ESD Human Body Model	JESD22-A114	2000V	1	0 / 9 (Pass)	1, 2
fication T	ESD Charged Device Model	JESD22-C101	1000V	1	0 / 3 (Pass)	1, 2
Electrical Verification Tests	Latch-Up (I-test) - Test at 105°C	JESD78	±200mA	1	0 / 6 (Pass)	1
Elec	Latch-Up (Overvoltage) - Test at 105°C		3V	1	0 / 3 (Pass)	1, 3

Note:

- 1) All electrical tests at different temperatures are performed before and after each item.
- 2) HBM & CDM tests are performed at room temp.
- 3) 3V is applied for VDD/VDDQ.