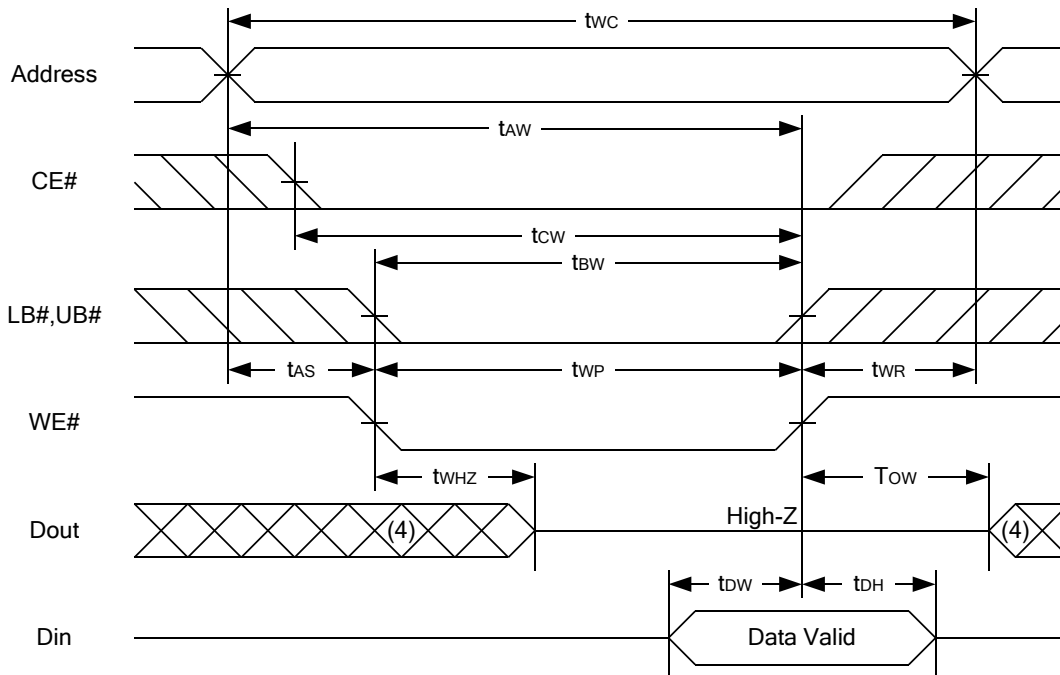


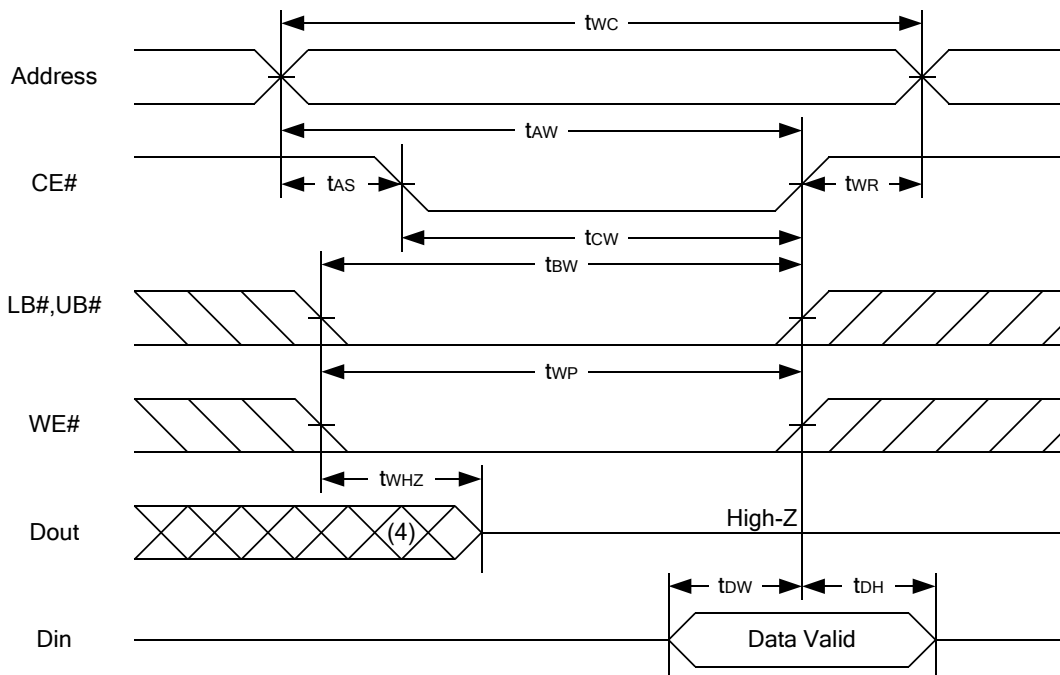
REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Nov.19.2008
Rev. 1.1	Revised <u>FEATURES & ORDERING INFORMATION</u> <u>Lead free and green package available to Green package available</u> Added packing type in <u>ORDERING INFORMATION</u> Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUM RATINGS</u> Revised <u>PACKAGE OUTLINE DIMENSION</u> in page 11 Revised V _{DR} to 1.5V	May.6.2010
Rev. 1.2	Revised <u>ORDERING INFORMATION</u> in page 12	Aug.30.2010
Rev. 1.3	Revised typo in <u>PRODUCT FAMILY</u> page 1	Oct.4.2010
Rev. 1.4	Deleted E Grade	Aug.9.2011
Rev. 1.5	Revised typo page 0 ABSOLUTE MAXIMUM RATINGS Revised typo Page 3 - ABSOLUTE MAXIMUM RATINGS Revised Page 12 - Package option from T(TSOPII) to Z (TSOP II)	Sep 29 2015

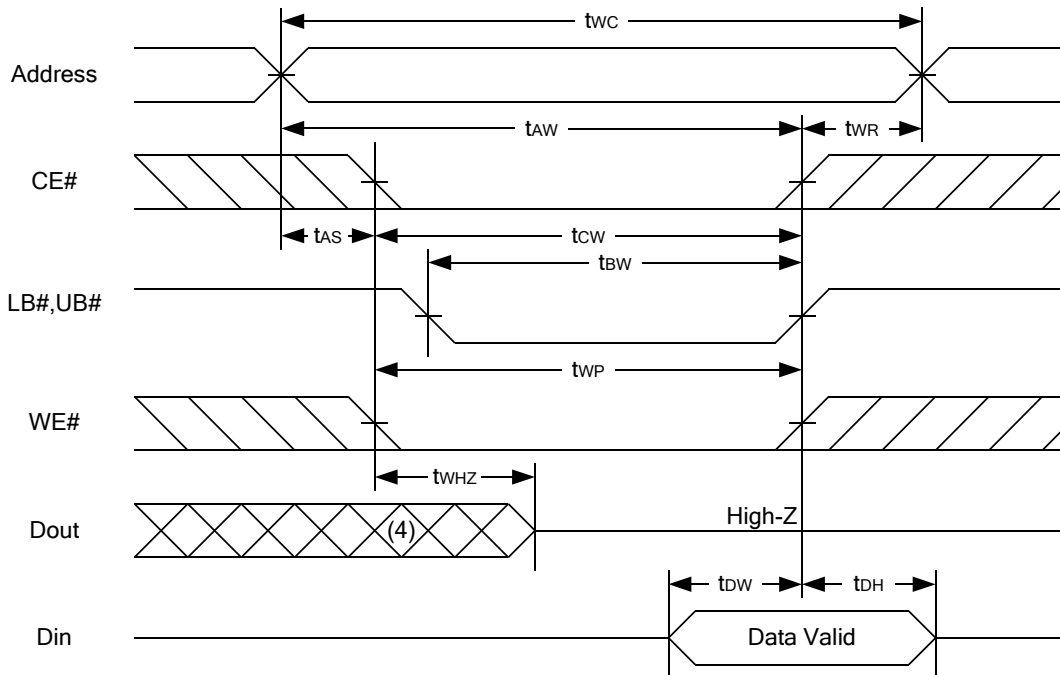
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



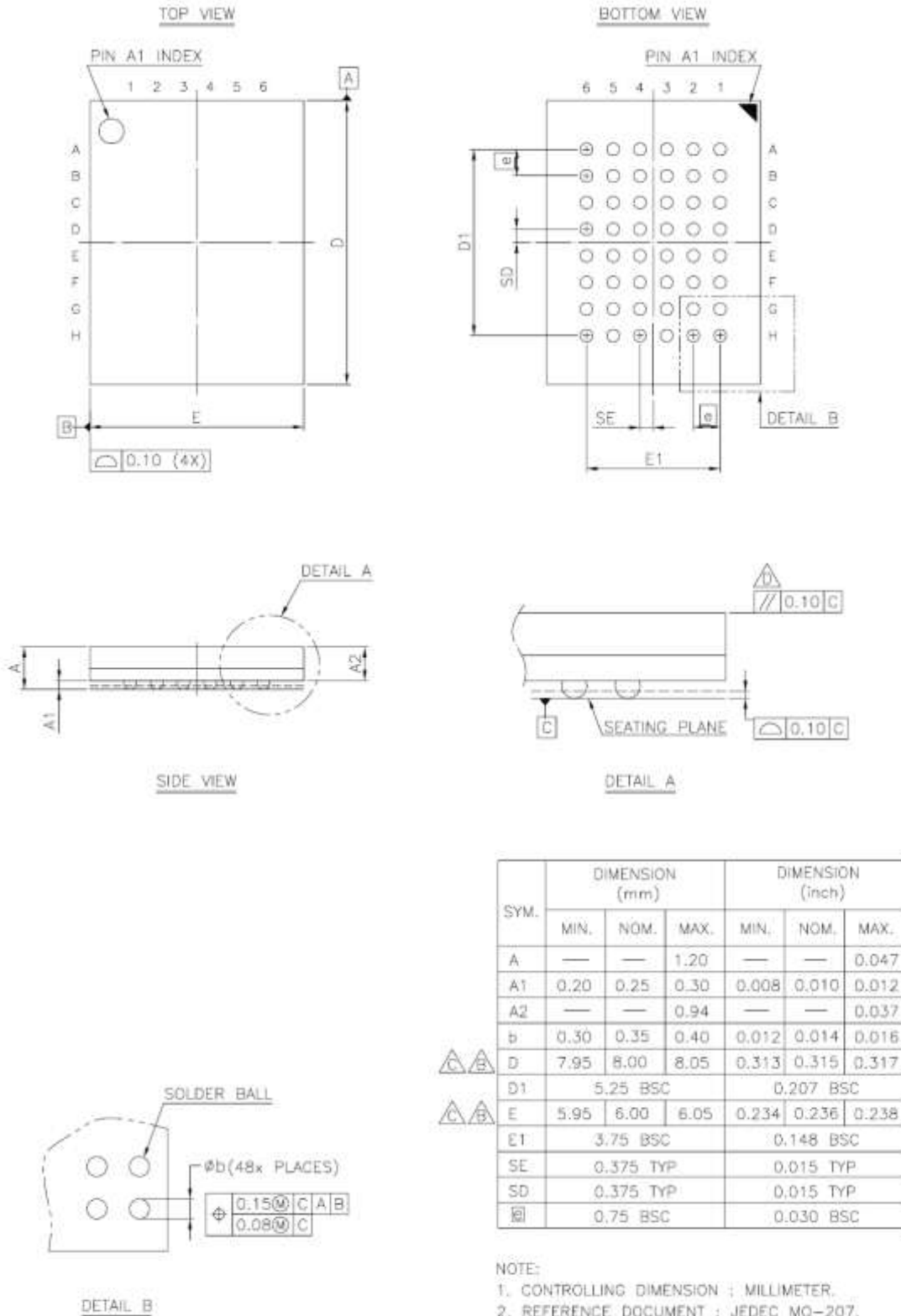
WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.

48-ball 6mm × 8mm TFBGA Package Outline Dimension



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